1. (30 points) Microcontroller system is using 8MHz crystal connected to XIN input and 3V power supply.

The DCO generator is connected to pin P2.5/Rosc if DCOR control bit is set.
The port pin P2.5/Rosc is selected if DCOR control bit is reset (initial state).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(DCO03)</td>
<td>( R_{\text{sel}} = 0, \text{DCO} = 3, \text{MOD} = 0, \text{DCOR} = 0, T_A = 25^\circ \text{C} )</td>
<td>( V_{CC} = 2.2 \text{ V} )</td>
<td>0.08</td>
<td>0.22</td>
<td>0.25</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3 \text{ V} )</td>
<td>0.08</td>
<td>0.13</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO13)</td>
<td>( R_{\text{sel}} = 1, \text{DCO} = 3, \text{MOD} = 0, \text{DCOR} = 0, T_A = 25^\circ \text{C} )</td>
<td>( V_{CC} = 2.2 \text{ V} )</td>
<td>0.14</td>
<td>0.22</td>
<td>0.25</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3 \text{ V} )</td>
<td>0.24</td>
<td>0.13</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO23)</td>
<td>( R_{\text{sel}} = 2, \text{DCO} = 3, \text{MOD} = 0, \text{DCOR} = 0, T_A = 25^\circ \text{C} )</td>
<td>( V_{CC} = 2.2 \text{ V} )</td>
<td>0.14</td>
<td>0.22</td>
<td>0.25</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3 \text{ V} )</td>
<td>0.25</td>
<td>0.13</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO33)</td>
<td>( R_{\text{sel}} = 3, \text{DCO} = 3, \text{MOD} = 0, \text{DCOR} = 0, T_A = 25^\circ \text{C} )</td>
<td>( V_{CC} = 2.2 \text{ V} )</td>
<td>0.14</td>
<td>0.22</td>
<td>0.25</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3 \text{ V} )</td>
<td>0.25</td>
<td>0.13</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO43)</td>
<td>( R_{\text{sel}} = 4, \text{DCO} = 3, \text{MOD} = 0, \text{DCOR} = 0, T_A = 25^\circ \text{C} )</td>
<td>( V_{CC} = 2.2 \text{ V} )</td>
<td>0.14</td>
<td>0.22</td>
<td>0.25</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 3 \text{ V} )</td>
<td>0.25</td>
<td>0.13</td>
<td>0.16</td>
<td>MHz</td>
</tr>
</tbody>
</table>
Set the following modes of operation:

a) (15 points) DC generated MCLK to 750 KHz, SMCLK to 93.75 KHz.

BCSCTL1: 0x\text{__} = \begin{array}{cccccccc}
1 & 0 & 0 & 0 & 0 & 1 & 1 \\
\text{XT2Off} & \text{XTS} & \text{DIVA}.1 & \text{DIVA}.0 & \text{XT5V} & \text{Rsel2} & \text{Rsel1} & \text{Rsel0}
\end{array}

BCSCTL2: 0x\text{__} = \begin{array}{cccccccc}
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
\text{SELM}.1 & \text{SELM}.0 & \text{DIVM}.1 & \text{DIVM}.0 & \text{SELS} & \text{DIVS}.1 & \text{DIVS}.0 & \text{DCOR}
\end{array}

DCOCTL: 0x\text{__} = \begin{array}{cccccccc}
0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\
\text{DCO}.2 & \text{DCO}.1 & \text{DCO}.0 & \text{MOD}.4 & \text{MOD}.3 & \text{MOD}.2 & \text{MOD}.1 & \text{MOD}.0
\end{array}

b) (15 points) Processor clock to 8MHz, ACLK to 4MHz.

BCSCTL1: 0x\text{__} = \begin{array}{cccccccc}
1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\
\text{XT2Off} & \text{XTS} & \text{DIVA}.1 & \text{DIVA}.0 & \text{XT5V} & \text{Rsel2} & \text{Rsel1} & \text{Rsel0}
\end{array}

BCSCTL2: 0x\text{__} = \begin{array}{cccccccc}
1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\
\text{SELM}.1 & \text{SELM}.0 & \text{DIVM}.1 & \text{DIVM}.0 & \text{SELS} & \text{DIVS}.1 & \text{DIVS}.0 & \text{DCOR}
\end{array}

DCOCTL: 0x\text{__} = \begin{array}{cccccccc}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\text{DCO}.2 & \text{DCO}.1 & \text{DCO}.0 & \text{MOD}.4 & \text{MOD}.3 & \text{MOD}.2 & \text{MOD}.1 & \text{MOD}.0
\end{array}

\textbf{NOTE:}
- XT5V bit should be 0.
- DCOR: use internal Rosc
- For all DIV fields:

\begin{array}{cccc}
\text{DIV field value} & 0 & 1 & 2 & 3 \\
\text{Divided by:} & 1 & 2 & 4 & 8
\end{array}
2. (15 points)
a) (5 points) What is the state (High/Low) of 68K signal lines for the following operations?

Solution:

<table>
<thead>
<tr>
<th>Operation</th>
<th>Word read</th>
<th>Byte read, Even address</th>
<th>Byte write, Odd address</th>
</tr>
</thead>
<tbody>
<tr>
<td>AS*</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>R/W*</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>UDS*</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>LDS*</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

b) (5 points) Describe the 68000’s read cycle explaining the actions that take place and the relationship between them. Give the simplified timing diagram.

| State S0  | R/W*output is set high to terminate any previous write cycle. |
| State S1  | The 68000 puts the address on the address bus. It remains valid for the duration of the read cycle. |
| State S2  | The 68000 asserts AS* and LDS*/UDS* to indicate that the address is valid. |
| State S3  | No signals change state. |
| State S4  | DTACK* must go low before the end of S4, if wait states are not required. |
| State S5  | No signals change state. |
| State S6  | Data from the memory is latched by the 68000 at the end of S6 state. |
| State S7  | The address and data strobes are de-asserted to terminate the read cycle. |
c) (5 points) Describe the 68000’s write cycle explaining the actions that take place and the relationship between them. Give the simplified timing diagram.
3. (55 points) Design a microcomputer system with a MC68000 microprocessor that features
   1) 256KB of supervisor program memory residing at the address $04000 using 32K×8 EPROMs modules
   2) 64KB of supervisor data memory using 4K×8bit static RAM modules, and
   3) 128KB of user program and data memory using 32K×8bit static RAM modules.
All three memories reside in consecutive address windows. Design necessary logic to generate:
- Address decoding signals (CS*)
- Control signals (WE*, OE*)
Tie all OE* low. OR the CS and the R/W* to generate WE* for each chip.

The memory map follows:

<table>
<thead>
<tr>
<th>Memory</th>
<th>Address Range</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPM</td>
<td>00 4000</td>
<td>0000 0000 0100 0000 0000 0000</td>
</tr>
<tr>
<td></td>
<td>+3 FFFF</td>
<td>0100 1111 1111 1111</td>
</tr>
<tr>
<td>SDM</td>
<td>04 3FFF</td>
<td>0100 0100 0100 0000 0000 0000</td>
</tr>
<tr>
<td></td>
<td>+0 FFFF</td>
<td>0101 1111 1111 1111</td>
</tr>
<tr>
<td>UPDM</td>
<td>05 4000</td>
<td>0101 0100 0100 0000 0000 0000</td>
</tr>
<tr>
<td></td>
<td>+1 FFFF</td>
<td>0110 1111 1111 1111</td>
</tr>
</tbody>
</table>

The address decoding for the supervisor program memory is as follows:

```
<table>
<thead>
<tr>
<th>A17-A1</th>
<th>A15-A1</th>
<th>A13-A1</th>
<th>A11-A9</th>
<th>A8-A0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPM</td>
<td>SPM</td>
<td>SPM</td>
<td>SPM</td>
<td>SPM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

---

**Diagram:**

- [Diagram of memory address decoding for SPM]
The address decoding for the user program and data memory is as follows:

The address decoding for the supervisor data memory is as follows: