1. (30 points) A MSP430 microcontroller system is using a 32KHz crystal connected to the LFXT1 Oscillator, an 8MHz crystal connected to the XT2 Oscillator, and a 3V power supply. See Appendix (pages 6-9) for necessary information.

Datasheet specifications:
\[
\frac{f_{\text{Resel}+1}}{f_{\text{Resel}}} = 1.65, \\
\frac{f_{\text{DCO}+1}}{f_{\text{DCO}}} = 1.12, \\
\text{DCOR: use internal } R_{\text{osc}}
\]

Set the following modes of operation (If the bit can be either 0 or 1, put d):

a) (10 points) processor clock (MCLK) to 2 MHz, ACLK to 16 KHz, SMCLK to 180 KHz.

b) (10 points) processor clock to 590 KHz, SMCLK to 295 KHz, and ACLK to 4 KHz.
c) (10 points) What should be the value of MOD if MCLK needs to be set to 2.6 MHz for the system that doesn’t use external oscillators (uses only DCO)? Give values for Rsel, DCO, and MOD. Show how you came up with the result. [Hint: use the formula \( T = ((32 - \text{MOD}) \times T_{\text{DCO}} + \text{MOD} \times T_{\text{DCO}+1})/32 \)]
2. (45 points) Using given memory components, design a memory subsystem for an MC68000-based microcomputer system with the following characteristics:
   a. 128 KB of supervisor program memory (EPROM) residing at address $000000
   b. 128 KB of supervisor data memory (out of 16K RAM) residing in the consecutive address window, and
   c. 64 KB of user program/data memory (out of 32K RAM) beginning at the address $080000.

Use LS138 decoder(s) (3 to 8) plus any other logic gates for address decoding, and generate:
- Address decoding signals (CS*)
- Control signals (WE*, OE*)

Use FC0-FC2 signals to make sure that memory is properly accessed. Make sure that the 68000 has access to user program and data space in supervisor mode.

<table>
<thead>
<tr>
<th>Function Code Output</th>
<th>Processor Cycle Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC2</td>
<td>FC1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
3. (20 points) A microcontroller system operates with a system frequency of 200 Hz (repeat the following sequence: a/d conversion, process data, real-time clock, idle). What is the expected system operation time if the system is supplied with 720mAh capacity battery? The power consumption of different components is:
- Analog interface circuit 1 mA, cycle operation time - 300 µs.
- Microcontroller in active mode 420 µA, cycle processing time:
  - 50 µs with probability 25%
  - 75 µs with probability 50%
  - 140 µs with probability 25%
- Microcontroller in idle mode 1.8 µA.
- Real Time Clock 300 µA, cycle operation time - 90 µs.
- LCD display 20 µA, always active.

4. (1 point) The ability to use different addressing modes for both source and destination is referred to as instruction ____________________.

5. (2 points) The MSP430 supports ________ addressing modes for source operands and ________ addressing modes for destination operands.

6. (2 points) _______________________ and ______________________________ are two addressing modes used in the MSP430.
# Appendix

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(DDC003)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.08</td>
<td>0.12</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC013)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.14</td>
<td>0.19</td>
<td>0.23</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC023)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.14</td>
<td>0.18</td>
<td>0.22</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC033)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.08</td>
<td>0.12</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC043)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.14</td>
<td>0.19</td>
<td>0.23</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC053)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.14</td>
<td>0.18</td>
<td>0.22</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC063)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.08</td>
<td>0.12</td>
<td>0.16</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC073)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.14</td>
<td>0.19</td>
<td>0.23</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC083)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.14</td>
<td>0.18</td>
<td>0.22</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DDC093)</td>
<td>VCC = 2.2 V, VCC = 3 V</td>
<td>0.08</td>
<td>0.12</td>
<td>0.16</td>
<td>MHz</td>
</tr>
</tbody>
</table>

## Diagram

![Diagram](image)

The DCO generator is connected to pin P2.5/Rosc if DCOR control bit is set. The port pin P2.5/Rosc is selected if DCOR control bit is reset (initial state).
7.5 Basic Clock Module Control Registers

The Basic Clock Module is configured using control registers DCOCTL, BCSCTL1, and BCSCTL2, and four bits from the CPU status register: SCG1, SCG0, OscOff, and CPUOFF. User software can modify these control registers from their default condition at any time. The Basic Clock Module control registers are located in the byte-wide peripheral map and should be accessed with byte (.B) instructions.

<table>
<thead>
<tr>
<th>Register</th>
<th>Short Form</th>
<th>Register Type</th>
<th>Address</th>
<th>Initial State</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCO control register</td>
<td>DCOCTL</td>
<td>Read/write</td>
<td>056h</td>
<td>060h</td>
</tr>
<tr>
<td>Basic clock system control 1</td>
<td>BCSCTL1</td>
<td>Read/write</td>
<td>057h</td>
<td>084h</td>
</tr>
<tr>
<td>Basic clock system control 1</td>
<td>BCSCTL2</td>
<td>Read/write</td>
<td>058h</td>
<td>reset</td>
</tr>
</tbody>
</table>
7.5.1 Digitally-Controlled Oscillator (DCO) Clock-Frequency Control

DCOCTL is loaded with a value of 060h with a valid PUC condition.

<table>
<thead>
<tr>
<th>DCOCTL</th>
<th>DC0.2</th>
<th>DC0.1</th>
<th>DC0.0</th>
<th>MOD.4</th>
<th>MOD.3</th>
<th>MOD.2</th>
<th>MOD.1</th>
<th>MOD.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>056h</td>
<td>rw-0</td>
<td>rw-1</td>
<td>rw-1</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>nw-0</td>
</tr>
</tbody>
</table>

MOD.0..MOD.4: The MOD constant defines how often the discrete frequency \( f_{DCO+1} \) is used within a period of 32 DCOCLK cycles. During the remaining clock cycles (32–MOD) the discrete frequency \( f_{DCO} \) is used. When the DCOconstant is set to seven, no modulation is possible since the highest feasible frequency has then been selected.

DC0.0 .. DC0.2: The DCO constant defines which one of the eight discrete frequencies is selected. The frequency is defined by the current injected into the dc generator.

7.5.2 Oscillator and Clock Control Register

BCSCTL1 is affected by a valid PUC or POR condition.

<table>
<thead>
<tr>
<th>BCSCTL1</th>
<th>XT2Off</th>
<th>XT5</th>
<th>DIVA.1</th>
<th>DIVA.0</th>
<th>XT5V</th>
<th>Rsel.2</th>
<th>Rsel.1</th>
<th>Rsel.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>057h</td>
<td>rw-(1)</td>
<td>rw-(0)</td>
<td>rw-(0)</td>
<td>rw-(0)</td>
<td>rw-1</td>
<td>nw-0</td>
<td>nw-0</td>
<td>nw-0</td>
</tr>
</tbody>
</table>

Bit0 to Bit2: The internal resistor is selected in eight different steps.

Rsel.0 to Rsel.2 The value of the resistor defines the nominal frequency.

The lowest nominal frequency is selected by setting Rsel=0.

Bit3, XT5V: XT5V should always be reset.

Bit4 to Bit5: The selected source for ACLK is divided by:

- \( \text{DIVA} = 0: 1 \)
- \( \text{DIVA} = 1: 2 \)
- \( \text{DIVA} = 2: 4 \)
- \( \text{DIVA} = 3: 8 \)

Bit6, XTS: The LFXT1 oscillator operates with a low-frequency clock crystal or with a high-frequency crystal:

- \( \text{XTS} = 0: \) The low-frequency oscillator is selected.
- \( \text{XTS} = 1: \) The high-frequency oscillator is selected.

The oscillator selection must meet the external crystal’s operating condition.

Bit7, XT2Off: The XT2 oscillator is switched on or off:

- \( \text{XT2Off} = 0: \) the oscillator is on
- \( \text{XT2Off} = 1: \) the oscillator is off if it is not used for MCLK or SMCLK.

BCSCTL2 is affected by a valid PUC or POR condition.
Bit0, DCOR: The DCOR bit selects the resistor for injecting current into the dc generator. Based on this current, the oscillator operates if activated.

DCOR = 0: Internal resistor on, the oscillator can operate. The fail-safe mode is on.
DCOR = 1: Internal resistor off, the current must be injected externally if the DCO output drives any clock using the DCOCLK.

Bit1, Bit2: The selected source for SMCLK is divided by:

DIVS.1, DIVS.0 DIVS = 0: 1
DIVS = 1: 2
DIVS = 2: 4
DIVS = 3: 8

Bit3, SELS: Selects the source for generating SMCLK:
SELS = 0: Use the DCOCLK
SELS = 1: Use the XT2CLK signal (in three-oscillator systems) or LFXT1CLK signal (in two-oscillator systems)

Bit4, Bit5: The selected source for MCLK is divided by:

DIVM.0, DIVM.1 DIVM = 0: 1
DIVM = 1: 2
DIVM = 2: 4
DIVM = 3: 8

Bit6, Bit7: Selects the source for generating MCLK:
SELM.0, SELM.1 SELM = 0: Use the DCOCLK
SELM = 1: Use the DCOCLK
SELM = 2: Use the XT2CLK (x13x and x14x devices) or Use the LFXT1CLK (x11xx and x12xx devices)
SELM = 3: Use the LFXT1CLK