From the book,
10.1 (20 points) (a) & (b) for q s-a-0 and d s-a-1, 10.2 (20 points), 10.7 (10 points)

From other sources
(25 points) Design a hardware multiplier circuit(M) that computes the product of two, positive 2-bit binary numbers.

\[ \begin{array}{c}
A_0 \\
A_1 \\
B_0 \\
B_1 \\
\end{array} \quad \begin{array}{c}
M_0 \\
M_1 \\
M_2 \\
M_3 \\
\end{array} \]

\(A_1A_0\) represents one 2-bit number, \(B_1B_0\) represents the second 2-bit number and \(M_3M_2M_1M_0\) represents the 4-bit product. For example, if \(A_1A_0 = 10\) and \(B_1B_0 = 11\), then \(M_3M_2M_1M_0 = 0110\). Model your circuit by performing the following steps.

a. Develop a VHDL entity declaration for the multiplier.
b. Develop an algorithmic behavioral architectural body for the multiplier.
c. Simulate to verify the correctness of your model.

(25 points) Design a sequential circuit that converts a 4-bit Gray code into a 4-bit BCD code. The inputs and outputs are timed by the same system clock. Assume that the device receives a START pulse coincident with the left most bit of the Gray code. The remaining bits of the Gray code are received one bit at a time (from left to right). At the end of each 4-bit Gray code, the device outputs the corresponding 4-bit BCD code in parallel along with a DAV signal. The next input could start during the clock period following the last input bit or at any time after that. The device must have a RESET input that initializes the device to the correct starting state. The figure given shows a block diagram and sample timing diagram. Use the table below for the Gray and BCD codes.

<table>
<thead>
<tr>
<th>Decimal Digit</th>
<th>Gray Code</th>
<th>BCD Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>0001</td>
</tr>
<tr>
<td>2</td>
<td>0011</td>
<td>0010</td>
</tr>
<tr>
<td>3</td>
<td>0010</td>
<td>0011</td>
</tr>
<tr>
<td>4</td>
<td>0110</td>
<td>0100</td>
</tr>
<tr>
<td>5</td>
<td>1110</td>
<td>0101</td>
</tr>
<tr>
<td>6</td>
<td>1010</td>
<td>0110</td>
</tr>
<tr>
<td>7</td>
<td>1011</td>
<td>0111</td>
</tr>
<tr>
<td>8</td>
<td>1001</td>
<td>1000</td>
</tr>
<tr>
<td>9</td>
<td>1000</td>
<td>1001</td>
</tr>
</tbody>
</table>

Model the device and do a simulation to verify your model.
SGTBCD
SI
RESET
CLOCK

CLOCK
START
SI
DAV
BCD

0101 0000
0000