1. (10 points) A sequential network consists of a PLA and a D flip-flop, as shown. The propagation delay for the PLA is in the range 5 to 10 ns, and the propagation delay from clock to output of the D flip-flop is 5 to 10 ns. Assuming that X always changes at the same time as the falling edge of the clock, what is the maximum setup and hold time specifications that the flip-flop can have and still maintain proper operation of the network?

2. (10 points) Write a short VHDL description of a 4-to-1 multiplexer using a VHDL process.

```
entity MUX4_1 is
    port (I3, I2, I1, I0, S1, S0 : in bit;
          F : out bit);
end MUX4_1;

architecture MUX4_1of MUX4_1is
begin
```

end MUX4_1;
3. (15 points) For the following VHDL, assume that A changes to ‘1’ at 5 ns. Give the values of A, B, C, D, E, and F each time a change occurs. Carry this out until no further change occurs. I

entity prob is
    port (D : inout bit);
end prob;

architecture PROB of PROB is
    signal A, B, C, E, F : bit;
begin
    P1: process (A, C)
    begin
        B <= A after 3 ns;
        E <= C after 5 ns;
    end process P1;
    C <= A after 10 ns;
    P2: process (C, E)
    begin
        F <= C and E after 4 ns;
    end process P2;
    D <= A or B or C or F after 1 ns;
end PROB;

<table>
<thead>
<tr>
<th>Time</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 ns</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5 ns</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

4. (5 points) Obtain a minimum product of sums expression for the following function:

\[ f(A, B, C, D) = \Pi M(0, 1, 2, 4, 5, 8, 9, 10) \]
5. (15 points) A Mealy sequence detector detects a sequence of four consecutive 1 inputs. The
detector has a single binary input, X, and a single binary output, Z. Signal Z should be logic 1 if
and only if the last four inputs were all logic 1. Here is an example input-output sequence:

<table>
<thead>
<tr>
<th>X</th>
<th>010111111011011110</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z</td>
<td>000000111100000000010</td>
</tr>
</tbody>
</table>

Derive a Mealy state graph and table with a minimum number of states for this sequence detector.

6. (10 points) For the following $F_t$, find all static-1 hazards. For each hazard, specify the values of
the input variables and which variable is changing when the hazard occurs.

$$F_t = ab' + ac' + bb' + bc' + a'd'$$
7. (10 points) Reduce the following state table to a minimum number of states. Show all your work in determining the state equivalents.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>X = 0</th>
<th>X = 1</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>I</td>
<td>C</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>B</td>
<td>I</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>C</td>
<td>G</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>D</td>
<td>I</td>
<td>C</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>E</td>
<td>D</td>
<td>E</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>F</td>
<td>I</td>
<td>C</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>G</td>
<td>E</td>
<td>F</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>A</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>I</td>
<td>A</td>
<td>C</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
8. (5 points) Write out the truth table for the following equation.
   \[ F = (A \cdot B') + C \]

9. (5 points) Draw a timing diagram that illustrates the difference between a D flip-flop and a D latch.

10. (1 point) ________________ design is a technique that uses a clock to coordinate the operation of all flip-flops, registers and counters in the system.

11. (1 point) The value of a ________________ changes instantaneously in VHDL.

12. (1 point) A process with a sensitivity list is activated whenever ________________.

13. (1 point) VHDL is case-sensitive (True/False) ____________

14. (1 point) ________________ networks commonly use flip-flops as storage devices.
15. (10 points) Draw the state diagram for the following state machine. Is it a Moore machine or a Mealy machine?

ENTITY state_machine IS
  PORT (sig_in : IN BIT; clk : IN BIT;
         sig_out : OUT BIT);
END state_machine;

ARCHITECTURE state_machine OF state_machine IS
  TYPE state_type IS (a, b, c, d, e);
  SIGNAL current_state, next_state : state_type;
BEGIN
  PROCESS (sig_in, current_state)
  BEGIN
    sig_out <= '0'; next_state <= b;
    CASE current_state
    WHEN a =>
      IF sig_in = '0' THEN next_state <= e; sig_out <= '1';
      ELSE next_state <= d;
      END IF;
    WHEN b =>
      IF sig_in = '0' THEN next_state <= b;
      ELSE next_state <= d; sig_out <= '1';
      END IF;
    WHEN c =>
      IF sig_in = '1' THEN next_state <= a;
      ELSE next_state <= d;
      END IF;
    WHEN d =>
      IF sig_in = '0' THEN next_state <= e;
      END IF;
    WHEN e =>
      IF sig_in = '1' THEN next_state <= a;
      END IF;
    END CASE;
  END PROCESS;
  PROCESS (clk)
  BEGIN
    IF (clk'EVENT AND clk = '1') THEN
      current_state <= next_state;
    END IF;
  END PROCESS;
END state_machine;

Extra Credit (5 points): Rework problem 6 using a Moore machine.