

CPE 426/526

Chapter 2 – Design Tools

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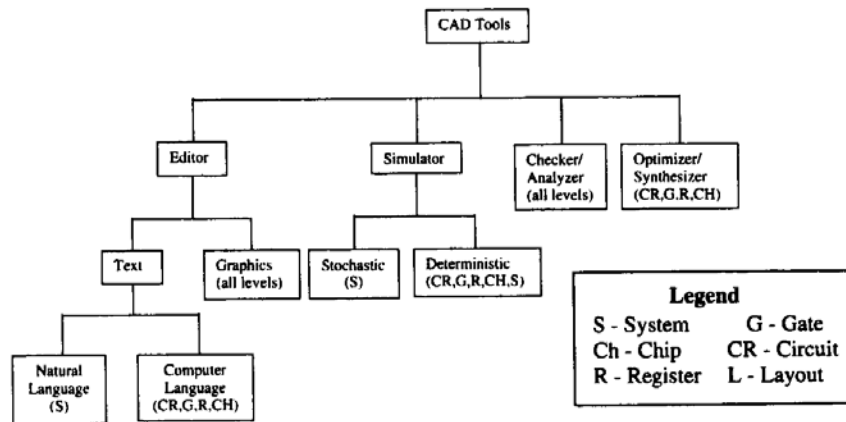
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Chapter 2

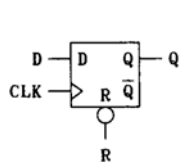
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2.1 CAD Tool Taxonomy

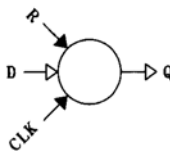


2.3 Simulators – Modeling Elements

- A _____ is a major modeling element in VHDL. The correspondence between _____ and _____ can be _____, _____, or _____.
- Example #1



(a) Digital device



(b) Graphical representation

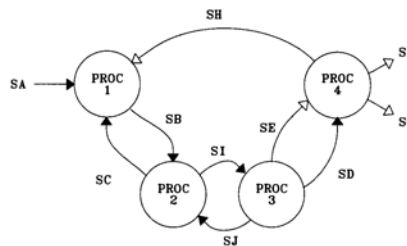
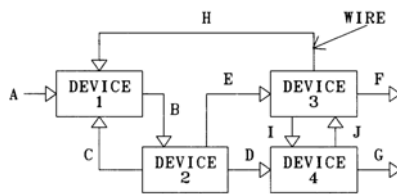
```

process (CLK, R)
begin
  if R='0'
    then q <= '0';
  elsif CLK'EVENT and CLK='1'
    then Q <= D;
  end if;
end process;
    
```

(c) VHDL process

2.3 Simulators – More About Modeling Elements

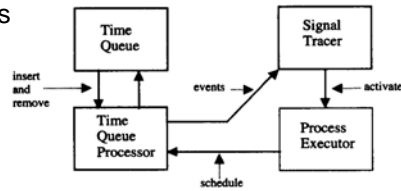
- Example #2



- There is also a correspondence between _____ and _____.
- A process is activated when a triggering signal _____, Non-triggering, or _____, signals do not cause activation and are represented graphically by using an _____.
- Signal _____ consist of a _____ and a _____ at which that _____ is scheduled to occur (SN, V). When a value on a signal changes, that is a _____ (processes are triggered by these).

2.4 Simulators – The Simulation System

- The simulation process proceeds as follows:
 - Initialization
 - While there are new time queue entries
 - For each current signal event
 - Trigger the appropriate process
 - Execute activated processes
- Simulator Organization
- Language Scheduling Mechanisms
- Simulation Efficiency
- A complete system consists of
 - Analysis -
 - Elaboration -



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2.5 Simulation Aids

- Model Preparation
 - Straight textual entry
 - Graphical entry
 - State diagram
 - Flow chart
- Model Test Vector Development
 - Manual
 - Graphical
 - Read from file
 - Macros in simulator
- Model Debugging
 - VHDL analyzers do range checking
 - Graphical debuggers are part of the simulation environment

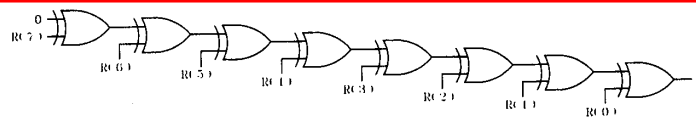
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2.7 Synthesis Tools

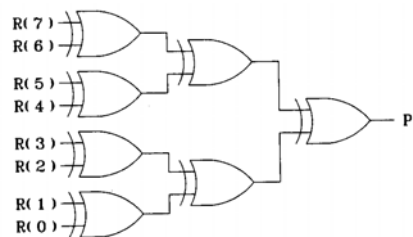
- Current tools work primarily at the register level of abstraction



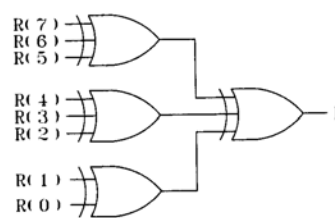
2.7 Synthesis Tools – Possible Synthesis Results



(a) Direct translation to iterative network.



(b) Optimization for 2-input XOR gates at maximum speed.



(c) Maximum speed implementation using 2 and 3 input XOR gates