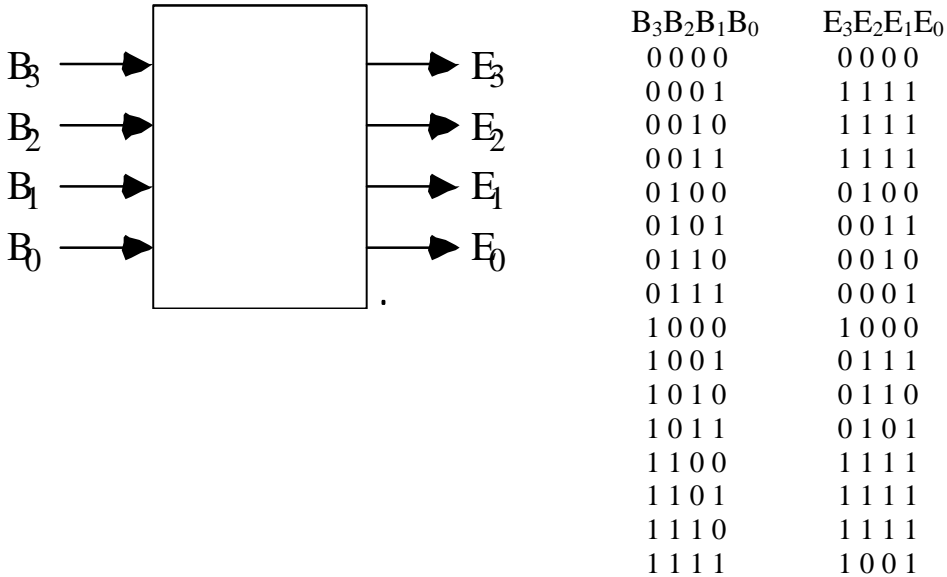


**The University of Alabama in Huntsville**  
**Electrical & Computer Engineering**  
**CPE 426/526**  
**January 21, 2009**  
**Homework #1**

**Due January 28, 2009**

Consider a code converter circuit that converts BCD 84-2-1 to BCD 8421.



$B_3B_2B_1B_0$  represents the 4-bit BCD 84-2-1 input and  $E_3E_2E_1E_0$  represents the 4-bit BCD 8421 output. For invalid BCD 84-2-1 inputs, all 1s are output as an error indication. You will find the following files on the web site.

- a. A VHDL entity declaration for the converter.
- b. An algorithmic behavioral architectural body for the converter.
- c. A data flow behavioral architectural body for the converter.
- d. A structural architectural body for the converter.
- e. A test bench entity that ties the entity to a pulse generator that generates all possible combinations of the inputs.
- f. Three configuration files
  - i. Test bench for the behavioral architecture
  - ii. Test bench for the dataflow architecture
  - iii. Test bench for the structural architecture

Perform the following steps

- a. Create a project in modelsim which has all these files
- b. Compile all of the files
- c. Simulate all three configurations to verify correctness.
- d. Save wave and list files for each simulation

Turn in your wave and list files.