

The University of Alabama in Huntsville
Electrical & Computer Engineering
CPE 426/526
Spring 2009
Homework #4

Due March 30, 2009

Consider the control for a washing machine that is synchronous with clock CK. The circuit has three external inputs, START, FULL, and EMPTY (which are 1 for at most a single clock cycle and are mutually exclusive) and external outputs, HOT, COLD, DRAIN, and TURN. The datapath for the control consists of a down-counter, which has three control inputs, REST, DEC, and LOAD and a data input COUNT. This counter synchronously decrements once each minute for DEC = 1, but can be loaded or synchronously reset on any cycle of clock CK. It has a single output, ZERO, which is 1 whenever the counter contains value zero and 0 otherwise. In its operation, the circuit goes through four distinct cycles, WASH, SPIN_1, RINSE, and SPIN_2 which are detailed as follows:

WASH: Assume that the circuit is in its power-up state IDLE. If START is 1 for a clock cycle, HOT becomes 1 and remains 1 until FULL = 1, filling the washer with hot water. Next, using LOAD, the down-counter is loaded with a value from a panel dial which indicates how many minutes the wash cycle is to last. DEC and TURN then become 1 and the washer washes its contents. When ZERO becomes 1, the wash is complete, and TURN and DEC become 0.

SPIN_1: Next, DRAIN becomes 1, draining the wash water. When EMPTY becomes 1, the down-counter is loaded with 7. DEC and TURN then become 1 and the remaining wash water is wrung from the contents. When ZERO becomes 1, DRAIN, DEC, and TURN return to 0.

RINSE: Next, COLD becomes 1 and remains 1 until FULL = 1, filling the washer with cold rinse water. Next, using LOAD, the down-counter is loaded with value 10. DEC and TURN then become 1 and the washer rinses its contents. When ZERO becomes 1, the rinse is complete, and TURN and DEC become 0.

SPIN_2: Next, DRAIN becomes 1, draining the rinse water. When EMPTY becomes 1, the down-counter is loaded with 8. DEC and TURN then become 1 and the remaining rinse water is wrung from the contents. When ZERO becomes 1, DRAIN, DEC, and TURN return to 0 and the circuit returns to state IDLE.

Turn in your VHDL source files and SDF files.

- (a) Write a VHDL model for the washing machine control.
- (b) Write a test bench to test your model. I will supply a text file.
- (c) Simulate to verify the correctness of your model.
- (d) Synthesize your model to an Altera FPGA using Quartus.
- (e) Place and route your design using Altera Quartus.
- (f) Write out the structural gate level VHDL and the SDF file.
- (g) Simulate the placed and routed design using ModelSim and your test bench.