2.1 CAD Tool Taxonomy

Legend
S - System    G - Gate
Ch - Chip     CR - Circuit
R - Register  L - Layout
2.3 Simulators – Modeling Elements

- A _______ is a major modeling element in VHDL. The correspondence between _______ and _______ can be ________, ________, or ________.

Example #1

```
process(CLK, R)
begin
  if R='0'
  then Q <= '0';
  elsif CLK'EVENT and CLK='1'
  then Q <= D;
  end if;
end process;
```

Example #2

- There is also a correspondence between _______ and _______.
- A process is activated when a triggering signal _______. Non-triggering, or _______, signals do not cause activation and are represented graphically by using an _________.
- Signal _______ consist of a _______ and a _______ at which that _______ is scheduled to occur (SN, V). When a value on a signal changes, that is a _________ (processes are triggered by these).
2.4 Simulators – The Simulation System

- The simulation process proceeds as follows:
  - Initialization
  - While there are new time queue entries
    - For each current signal event
    - Trigger the appropriate process
    - Execute activated processes

- Simulator Organization
- Language Scheduling Mechanisms

- Simulation Efficiency
- A complete system consists of
  - Analysis -
  - Elaboration -

2.5 Simulation Aids

- Model Preparation
  - Straight textual entry
  - Graphical entry
    - State diagram
    - Flow chart

- Model Test Vector Development
  - Manual
  - Graphical
  - Read from file
  - Macros in simulator

- Model Debugging
  - VHDL analyzers do range checking
  - Graphical debuggers are part of the simulation environment
2.7 Synthesis Tools

- Current tools work primarily at the register level of abstraction.

```vhdl
-- This example illustrates VHDL constructs that can be translated into an iterative network.

entity IPAR is
  generic (PROP_DEL:time);
  port (R: in BIT_VECTOR (7 downto 0); P: out BIT);
end IPAR;

-- Model using a FOR loop
architecture LOOP of IPAR is
begin
  process (K)
  variable X: BIT;
  begin
    X := 0;
    for I in 7 downto 0 loop
      X := X xor R(I);
    end loop;
    P <= X after PROP_DEL;
  end process;
end LOOP;
```

2.7 Synthesis Tools – Possible Synthesis Results

(a) Direct translation to iterative network.

(b) Optimization for 2-input XOR gates at maximum speed.

(c) Maximum speed implementation using 2 and 3 input XOR gates.