

**The University of Alabama in Huntsville**  
**Electrical & Computer Engineering**  
**CPE 426/526**  
**September 18, 2007**  
**Homework #2**

**Due September 25, 2007**

Consider a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

Develop the following items

- a. A VHDL entity declaration for the circuit.
- b. An algorithmic behavioral architectural body for the circuit.
- c. A data flow behavioral architectural body for the circuit.
- d. A structural architectural body for the circuit (Use 1 ns delay in each AND, OR, etc. gate).
- e. Three configuration files
  - i. Test bench for the behavioral architecture
  - ii. Test bench for the dataflow architecture
  - iii. Test bench for the structural architecture

Perform the following steps

- a. Modify the test bench given in homework #1 to test this circuit.
- b. Compile all of the files
- c. Simulate all three configurations to verify correctness.
- d. Save wave and list files for each simulation

Turn in your wave and list files.