

The University of Alabama in Huntsville
Electrical and Computer Engineering
Course Syllabus
CPE 426/526 01
Fall 2007

Textbook: VHDL Design Representation and Synthesis, James R. Armstrong and F. Gail Gray, Prentice Hall, 2000, Second Edition.

Web Page: <http://www.ece.uah.edu/courses/cpe526>

Instructor: Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573,
email: gaede@ece.uah.edu

Office Hours: M 2 PM – 4 PM, W 10 AM – 12 PM, R 4 PM – 5 PM, F 8 AM – 9AM, or by appointment

<u>Grading:</u>	Homework	15 %
	Project	30 %
	Midterm	25 %
	Final Exam	25 %
	Class Attendance	5 %

Graduate Students will have extra and/or different problems on their tests. The grading for the project will be 1/3 for the project presentation and 2/3 for the project report. Attendance is calculated as follows: A student may miss up to 4 classes of the 28 classes in the semester and still receive all 5 points from attendance. If a student misses 5 or more classes, they receive 0 attendance points.

Homework: NO late homework will be accepted without extenuating circumstances. Contact me as soon as a problem occurs.

Important Dates: August 24 – Last day to add a class and file course repeat
September 3 – Holiday
August 31 – Last day to withdraw with refund
September 10 – Last day to apply for Pass/Fail
September 17 – Last day to change from credit to audit
October 11-12 – Fall Break
October 31 – Last day to withdraw
November 5 – Advising and registration for Spring 2008 begins
November 21-24 – No Classes
November 29 – Last TR class

Final Exam: Monday, December 3, 8:00 AM – 10:30 AM

Miscellaneous: Homework will be done individually.
Projects will be done in groups.
Mute your cell phones before you bring them to class.
Both a presentation and a written report are required for the project.

Course Outline:

Chapter	Topics
1	Structured Design Concepts The Abstraction Hierarchy, Textual vs. Pictorial Representations, Types of Behavioral Descriptions, Design Process, Structural Design Decomposition, The Digital Design Space
2	Design Tools CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools
3	Basic Features of VHDL Major Language Constructs, Lexical Descriptions, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93
4	Basic VHDL Modeling Techniques Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives
5	Algorithmic Level Design General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems
6	Register Level Design Transition from Algorithmic to Data Flow Descriptions, Timing Analysis
7	Gate Level and ASIC Library Modeling Accurate Gate Level Modeling, VITAL: A Standard for the Generation of VHDL Models of Library Elements Error Checking, Configuration Declarations for Gate Level Models, Approaches to Delay Control
8	HDL-Based Design Techniques Design of Combinational Logic Circuits, Design of Sequential Logic Circuits
9	ASICs and the ASIC Design Process What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis
10	Modeling for Synthesis Behavioral Model Development, The Semantics of Simulation and Synthesis, Modeling Sequential Behavior, Modeling Combinational Circuits for Synthesis, Inferred Latches and Don't Cares, Tristate Circuits, Shared Resources, Flattening and Structuring, Effect of Modeling Style on Circuit Complexity
12	Synthesis Algorithms for Design Automation Benefits of Algorithmic Synthesis, Algorithmic Synthesis Tasks, Scheduling Techniques, Allocation Techniques, State of the Art in High-Level Synthesis, Automated Synthesis of VHDL Constructs

I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook while I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

Name (Printed)

Signature

Date