

Getting Started with Design Analyzer

- Copy the file `.synopsys_dc.setup` file from the web site into your home directory.
- In the directory where your source files are, type `design_analyzer&` in the terminal to start design analyzer as a background process.
- Pull down the file menu and select Read.
- From the Read File dialog box, select the source file you wish to synthesize. If necessary, modify the file format by clicking, holding and selecting. Click OK.
- You will see a new window titled VHDL which tells you the result of this process. Any errors will be reported here. When this has completed, click on Cancel to go back to the main window.
- You will now see a design with the name of your entity. It has been synthesized into generic logic as an intermediate form to mapping to a target technology. The target technology we use in this class is `lsi_10k`. Click on it to select it. Use the down arrow from the palette in the left part of the window to push down into that design. You now see the ports on the entity. Use the AND gate icon from the palette to see the logic implementation.
- Pull down the Tools Menu and select Design Optimization. Click OK.
- You will see a new window titled Compile Log. When this process is complete, click on Cancel to take you back to the main window.
- You can now look at the result of the mapping to the `lsi_10k` library and the optimization.
- With your design selected, you can generate numerous reports by pulling down the Analysis menu and selecting Report.
- You will now see a dialog box with the title Report.
- Select Area and Timing. Select whether you want the output to go to the window or to a file. Change the file name, if necessary, then click on Apply.
- Click Cancel to dismiss the Report Output.
- To save the results of synthesis, pull down the file menu and select Save As. In the Save File dialog box, select a file format (DB is the native Synopsys format) and type in a file name, if desired.