

## Getting Started with MAX+plus II

- In the directory where you created your FPGA Compiler project, type `max2win&` in the terminal to start MAX+plusII as a background process. You may get a message saying MAX+plusII needs to enumerate some fonts. This can take a long time the first time it occurs.
- Select File from the pulldown menu and open your .edf file.
- Also, from the File pulldown, select Project -> Set Project to Current File.
- Close the window which shows your .edt file.
- Select Assign -> Device from the pulldown menu
- Select the FLEX10K Device Family and AUTO Devices and Click OK.
- Select MAX+Plus II -> Compiler from the pulldown menu.
- Select Interfaces -> EDIF Netlist Reader Settings from the pulldown menu and select Synopsys as the Vendor and Click OK.
- Select Interfaces -> VHDL Netlist Writer from the pulldown menu. You should now see a block titled VHDL Netlist Writer in your Compiler window. This is a toggle. You turn it off the same way.
- Select Interfaces -> VHDL Netlist Writer Settings from the pulldown menu. Select SDF Output File [.sdo] Ver 2.1 (VITAL) and Click OK.
- In the Compiler Window, Click Start.
- Watch the hourglass spin.
- When the Compiler reports that you have 0 errors and 0 warnings, rejoice and Click OK.
- You now have what you need to do your post place and route simulation. The SDF file has a .sdo extension and the structural gate-level VHDL file has a .vho extension.