14. Commonly used Compiler Directives

define word_size 32
include .header v
timescale 100ns/1ns
ifelse , else , endif
end
module and_op (a,b,c);
and a, b, c.
ifelse behavioral
  wire a = b & c;
else
  and a (b, c);
endif
endmodule

13. Observing Outputs
display ("Value of variable is ", var);
integer flag;
initial flag = ifopen("out_file");
always begin // dump data in test file
  $display (flag, ":", $data(7:0));
end
fclose ("out_file");

14. Simulation Control
initial begin
  $dumpfile("my_dump"); // dump in this file
  $dumpvars;
  $dumpvars (1.top); // dump variables in module instance top
  $dumpvars (2.top,m1);
  #1000 dumpoff;
  #600 dumpon;
  #1000 dumpoff;
  $finish;
end

15. Language Constructs not supported by most Synthesis tools

Declarations and Definitions
time declaration
event declaration
trind, trisc, trif, trio, and breg net types
primitive definition

Statements
initial statement
delay control
wait statement
repeat statement
fork statement
dezassign statement

2. Parallel Statements
Following statements start executing simultaneously inside module
initial begin // sequential statements
end
always begin // sequential statements
end
assign wire_name = expression;

3. Basic Data Types
a. Nets
  e.g. wire, wire, tri, nor
    - Continuously driven
    - Gets new value when driver changes
    - LHS of continuous assignments
      tri (15:0) data;
      // unconditional
      assign data[15:0] = data_in ;
      // conditional
      assign data[15:0] = enable ? data_in : 16'bz;

b. Registers
  e.g. reg
    - Represents storage
    - Always stores last assigned value
    - LHS of an assignment in procedural block
      reg signal;
      @ (posedge clock) signal[1'b1] = 1'b1; // positive edge
      @ (posedge clock) signal[1'b0]; // event (both edges)

4. Sequential Statements
Given below are simple examples instead of ENF type of definitions.
  if (reset == 0) begin
    data = #0; //
  end

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