

The University of Alabama in Huntsville  
Electrical & Computer Engineering Department  
CPE 426 01  
Final Exam  
April 30, 2002

Name: \_\_\_\_\_

1. (5 points) What kind of hardware element will be inferred by a synthesis tool from the following model?

```
library ieee;
use ieee.std_logic_1164.all;

entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK, RESET : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;

architecture EXAMPLE of WIDGET is
begin
  process (CLK, RESET)
  begin
    if (RESET = '1' then
      Z <= '0';
    elsif (CLK = '1') then
      Z <= A nor B;
    end if;
  end process;
end EXAMPLE;
```

2. (9 points) Draw the transistor-level diagram of a CMOS three-input NAND gate.

3. (12 points) Modify the following VHDL model by adding a parameter that sets the number of flip-flops in the counter. Also, add an input which is loaded with an asynchronous load input signal which is active low.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity UPCOUNT is
  port ( CLOCK, RESETN, E : in std_logic;
        Q : out std_logic_vector (3 downto 0));
end UPCOUNT;

architecture BEHAVIOR of UPCOUNT is
  signal COUNT : std_logic_vector (3 downto 0);
begin
  process (CLOCK, RESETN)
  begin
    if RESETN = '0' then
      COUNT <= "0000";
    elsif (CLOCK' event and CLOCK = '1') then
      if E = '1' then
        COUNT <= COUNT + 1;
      else
        COUNT <= COUNT;
      end if;
    end process
  Q <= COUNT;
```

Consider the following VHDL code:

```
-----  
-- Entity declaration  
-----  
  
entity SCHED2 is  
  port (A, B, C, D, E, F: in INTEGER;  
        CLK : in BIT;  
        W, X, Y: out INTEGER);  
end SCHED2;  
  
-----  
-- Architecture declaration  
-----  
  
architecture HIGH_LEVEL of SCHED2 is  
  signal Z: INTEGER;  
begin  
  X <= (A - B) * C * D;  
  Y <= (A * B) + (E + F)/D;  
  W <= (C + F) * B  
end HIGH_LEVEL;
```

4. (18 points) The following tasks refer to the VHDL code above. Assume that there are no hardware constraints.

- a. (6 points) Draw a data flow graph.

- b. (6 points) Derive an ASAP schedule.
- c. (6 points) Derive an ALAP schedule.

5. (10 points) Derive a schedule using the freedom-directed method for the VHDL code above, using the following hardware constraint; all operations are done in an ALU module and there are two ALU modules available.

6. (4 points) List the four types of paths that must be considered when doing timing analysis of sequential circuits.

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7. (10 points) For the data lifetime chart shown, use the left edge algorithm to obtain an efficient register allocation.

	A	B	C	D	E	F	G	H	I	J
S1			X	X						X
S2			X							X
S3			X				X			X
S4	X						X			X
S5	X						X			
S6	X	X				X				
S7	X	X				X				
S8		X				X		X		
S9		X						X	X	
S10		X			X			X	X	

8. (2 points) A(n) \_\_\_\_\_ is an integrated circuit produced for a specific application and produced in relatively small volumes.

9. (2 points) \_\_\_\_\_ is an annoyingly strongly typed language.

10. (15 points) Create a VHDL entity named mux4to1 that represents a 4-to-1 multiplexer which has an architecture which uses a case statement to represent the functionality of the multiplexer. Create a second entity and its accompanying architecture that represents a 16-to-1 decoder by using four instances of the mux4to1 entity.

11. (8 points) If the NRE costs for FPGA and CBIC circuits are \$25,000 and \$166,000, respectively, and the cost of individual parts for FPGA and CBIC circuits are \$20 and \$6, respectively, what is the break-even manufacturing volume for these two types of circuits?

12. (2 points) \_\_\_\_\_ are primitives that are all the same height and varying widths.

13. (3 points) The three types of primary design units are \_\_\_\_\_, \_\_\_\_\_, and \_\_\_\_\_.