

The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 526 01
Sample Final Exam
Spring 2002

Name: _____

1. (1 point) A(n) _____ file stores the timing data generated by EDA tools for use at any stage in the design process.
2. (1 point) _____ allow us to bind components in a structural model to the architecture and entity for that component.
3. (10 points) Modify the following VHDL model by adding a parameter that sets the number of flip-flops in the counter.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
entity UPCOUNT is
    port ( CLOCK, RESETN, E : in std_logic;
          Q : out std_logic_vector (3 downto 0));
end UPCOUNT;
```

```
architecture BEHAVIOR of UPCOUNT is
    signal COUNT : std_logic_vector (3 downto 0);
begin
    process (CLOCK, RESETN)
    begin
        if RESETN = '0' then
            COUNT <= '0000';
        elsif (CLOCK'event and CLOCK = '1') then
            if E = '1' then
                COUNT <= COUNT + 1;
            else
                COUNT <= COUNT;
            end if;
        end process
        Q <= COUNT;
    end BEHAVIOR;
```

4. (5 points) What kind of hardware element will be inferred by a synthesis tool from the following model?

```
library ieee;
use ieee.std_logic_1164.all;

entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;

architecture EXAMPLE of WIDGET is
begin
  process (CLK)
  begin
    if (CLK = '1') then
      Z <= A nor B;
    end if;
  end process;
end EXAMPLE;
```

5. (8 points) Draw the transistor-level diagram of a CMOS three-input NOR gate.

6. (2 points) Why does CMOS logic have low static-power dissipation?

7. (3 points) A modeler wishes to model a counter with an integer variable. Should he use type Integer or a constrained integer? Why?

Consider the following VHDL code:

```
-----  
-- Entity declaration  
-----  
  
entity SCHED2 is  
  port (A, B, C, D, E, F: in INTEGER;  
        CLK : in BIT;  
        X, Y: out INTEGER);  
end SCHED2;  
  
-----  
-- Architecture declaration  
-----  
  
architecture HIGH_LEVEL of SCHED2 is  
  signal Z: INTEGER;  
begin  
  X <= (A - B) * Z;  
  Y <= (A * B) + Z;  
  Z <= C * D + (E + F)/D;  
end HIGH_LEVEL;
```

8. (15 points) The following tasks refer to the VHDL code above. Assume that there are no hardware constraints.

- a. (5 points) Draw a data flow graph.
- b. (5 points) Derive an ASAP schedule.
- c. (5 points) Derive an ALAP schedule.

9. (10 points) Derive a schedule using the freedom-directed method for the VHDL code above, using the following hardware constraint; all operations are done in an ALU module and there are two ALU modules available.

10. (10 points) For the data lifetime chart shown, use the left edge algorithm to obtain an efficient register allocation.

	A	B	C	D	E	F	G	H	I	J	K	L
S1			X	X			X					
S2		X	X		X		X			X		
S3		X				X	X	X		X		
S4	X	X				X			X			X
S5	X					X			X		X	X

11. (10 points). Develop a VHDL model for an SN7400 2-input NAND gate. Use generics to represent T_{PHL} and T_{PLH}.

12. (15 points) Create a VHDL entity named if2to4 that represents a 2-to-4 binary decoder which has an architecture which uses an if-then-else statement to represent the functionality of the decoder. Create a second entity and its accompanying architecture that represents a 3-to-8 decoder by using two instances of the if2to4 entity.

13. (4 points) List the four types of paths which must be considered when doing timing analysis of sequential circuits.

14. (6 points) If the NRE costs for MPBA and CBIC circuits are \$97,000 and \$166,000, respectively, and the cost of individual parts for MPBA and circuits are \$9 and \$6, respectively, what is the breakeven manufacturing volume for these two types of circuits?