

CPE 426/526
Spring 2003
Final Exam Review

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VHDL Problem

```
use ieee.std_logic_unsigned.all;
entity UPCOUNT is
  port ( CLOCK, RESETN, E : in std_logic;
        Q : out std_logic_vector (3 downto 0));
end UPCOUNT;
architecture BEHAVIOR of UPCOUNT is
  signal COUNT : std_logic_vector (3 downto 0);
begin
  process (CLOCK, RESETN)
  begin
    if RESETN = '0' then
      COUNT <= "0000";
    elsif (CLOCK'event and CLOCK = '1') then
      if E = '1' then
        COUNT <= COUNT + 1;
      else
        COUNT <= COUNT;
      end if;
    end process; Q <= COUNT;
end BEHAVIOR;
```

Synthesis Style Question

```
entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK, RESET : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;
architecture EXAMPLE of WIDGET is
begin
  process (CLK, RESET)
  begin
    if (RESET = '0') then
      Z <= '000';
    elsif (CLK = '0') then
      Z <= A nor B;
    end if;
  end process;
end EXAMPLE;
```

Another Synthesis Style Question

```
entity WIDGET is
  Port (A, B : in SIGNED (0 to 2);
        CLK : in std_logic;
        Z : out SIGNED(0 to 2));
end WIDGET;
architecture EXAMPLE of WIDGET is
begin
  process (CLK)
  begin
    if (CLK = '1') then
      Z <= A nor B;
    end if;
  end process;
end EXAMPLE;
```

Scheduling Example

```
entity SCHED2 is
  port (A, B, C, D, E, F: in INTEGER;
        CLK : in BIT;
        W, X, Y: out INTEGER);
end SCHED2;

architecture HIGH_LEVEL of SCHED2 is
  signal Z: INTEGER;
begin
  X <= (A - B) * C * D;
  Y <= (A * B) + (E + F)/D;
  W <= (C + F) * B
end HIGH_LEVEL;
```

Scheduling Example-ALAP

```
entity SCHED2 is
  port (A, B, C, D, E, F: in INTEGER;
        CLK : in BIT;
        W, X, Y: out INTEGER);
end SCHED2;

architecture HIGH_LEVEL of SCHED2 is
  signal Z: INTEGER;
begin
  X <= (A - B) * C * D;
  Y <= (A * B) + (E + F)/D;
  W <= (C + F) * B
end HIGH_LEVEL;
```

Left Edge Algorithm

	A	B	C	D	E	F	G	H	I	J	K	L
S1			X	X			X					
S2	X	X			X		X			X		
S3		X				X	X	X		X		
S4	X	X				X			X			X
S5	X					X			X		X	X

	A	B	C	D	E	F	G	H	I	J	K	L
S1												
S2												
S3												
S4												
S5												

VHDL Modeling

- Design a resetting sequential majority function that asserts (active high) the output if the past three inputs contain two or more 1's. Assume a Moore machine.

Sample input/output sequences are given below.

- X = 0101110110
- Z = 0000010010

Implementation Medium Choice

If the NRE costs for FPGA and CBIC circuits are \$25,000 and \$166,000, respectively, and the cost of individual parts for FPGA and CBIC circuits are \$20 and \$6, respectively, what is the break-even manufacturing volume for these two types of circuits?

