

**The University of Alabama in Huntsville**  
**Electrical and Computer Engineering**  
**Course Syllabus**  
**CPE 426/526 01**  
**Spring 2005**

Textbook: VHDL Design Representation and Synthesis, James R. Armstrong and F. Gail Gray, Prentice Hall, 2000, Second Edition.

Web Page: <http://www.ece.uah.edu/courses/cpe526>

Instructor: Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573,  
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Office Hours: MW 2 PM – 3 PM, TR 4 PM – 5 PM, F 9 AM – 10 AM, or by appointment

<u>Grading:</u>	Homework	15 %
	Project	30 %
	Midterm	25 %
	Final Exam	25 %
	Class Attendance	5 %

Graduate Students will have extra and/or different problems on their tests. The grading for the project will be 1/3 for the project presentation and 2/3 for the project report. Attendance is calculated as follows: A student may miss up to 5 classes of the 28 classes in the semester and still receive all 5 points from attendance. If a student misses 6 or more classes, they receive 0 attendance points.

Homework: NO late homework will be accepted without extenuating circumstances.  
Contact me as soon as a problem occurs.

Important Dates: January 14 – Last day to add a class and file course repeat  
January 17 – Holiday  
January 24 – Last day to withdraw with refund  
January 31 – Last day to apply for Pass/Fail  
February 7 – Last day to change from credit to audit  
March 28 – Last day to withdraw  
March 21-26 – Spring Break  
April 4 – Advising and registration for Summer and Fall 2005 begins  
April 12 – Honors Day – No Classes  
April 26 – Last TR class  
April 26 – Last day to remedy an I from previous semester

Final Exam: Thursday, April 28, 3:00 PM – 5:30 PM

Miscellaneous: Homework will be done individually.  
Projects will be done in groups.  
Mute your cell phones before you bring them to class.  
Both a presentation and a written report are required for the project.

**Course Outline:**

Chapter	Topics
1	<b>Structured Design Concepts</b> The Abstraction Hierarchy, Textual vs. Pictorial Representations, Types of Behavioral Descriptions, Design Process, Structural Design Decomposition, The Digital Design Space
2	<b>Design Tools</b> CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools
3	<b>Basic Features of VHDL</b> Major Language Constructs, Lexical Descriptions, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93
4	<b>Basic VHDL Modeling Techniques</b> Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives
5	<b>Algorithmic Level Design</b> General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems
6	<b>Register Level Design</b> Transition from Algorithmic to Data Flow Descriptions, Timing Analysis
7	<b>Gate Level and ASIC Library Modeling</b> Accurate Gate Level Modeling, Error Checking, Multivalued Logic for Gate Level Modeling, Configuration Declarations for Gate Levels Models, Modeling Races and Hazards, Approaches to Delay Control
8	<b>HDL-Based Design Techniques</b> Design of Combinational Logic Circuits, Design of Sequential Logic Circuits
9	<b>ASICs and the ASIC Design Process</b> What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis
10	<b>Modeling for Synthesis</b> Behavioral Model Development, The Semantics of Simulation and Synthesis, Modeling Sequential Behavior, Modeling Combinational Circuits for Synthesis, Inferred Latches and Don't Cares, Tristate Circuits, Shared Resources, Flattening and Structuring, Effect of Modeling Style on Circuit Complexity
11	<b>Integration of VHDL into a Top-Down Design Methodology</b> Top-Down Design Methodology, Sobel Edge Detection Algorithm, System Requirements Level, System Definition Level, Architecture Design, Detailed Design at the RTL Level, Detailed Design at the Gate Level
12	<b>Synthesis Algorithms for Design Automation</b> Benefits of Algorithmic Synthesis, Algorithmic Synthesis Tasks, Scheduling Techniques, Allocation Techniques, State of the Art in High-Level Synthesis, Automated Synthesis of VHDL Constructs

I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook while I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

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Name (Printed)

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Signature

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Date