The University of Alabama in Huntsville
Electrical and Computer Engineering
Course Syllabus
CPE 426/526 01
Spring 2006


Web Page: http://www.ece.uah.edu/courses/cpe526

Instructor: Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573, email: gaede@ece.uah.edu

Office Hours: MW 2 PM – 3 PM, R 4 PM – 5 PM, or by appointment

Grading: Homework 15 %
Project 30 %
Midterm 25 %
Final Exam 25 %
Class Attendance 5 %

Graduate Students will have extra and/or different problems on their tests. The grading for the project will be 1/3 for the project presentation and 2/3 for the project report. Attendance is calculated as follows: A student may miss up to 4 classes of the 28 classes in the semester and still receive all 5 points from attendance. If a student misses 5 or more classes, they receive 0 attendance points.

Homework: NO late homework will be accepted without extenuating circumstances. Contact me as soon as a problem occurs.

Important Dates: January 13 – Last day to add a class and file course repeat
January 16 – Holiday
January 23 – Last day to withdraw with refund
January 30 – Last day to apply for Pass/Fail
February 6 – Last day to change from credit to audit
March 27 – Last day to withdraw
March 20-25 – Spring Break
April 4 – Advising and registration for Summer and Fall 2005 begins
April 11 – Honors Day – No Classes
April 25 – Last TR class
April 25 – Last day to remedy an I from previous semester

Final Exam: Thursday, April 27, 3:00 PM – 5:30 PM

Miscellaneous: Homework will be done individually.
Projects will be done in groups.
Mute your cell phones before you bring them to class.
Both a presentation and a written report are required for the project.
### Course Outline:

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<th>Chapter</th>
<th>Topics</th>
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| 1       | **Structured Design Concepts**  
| 2       | **Design Tools**  
CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools |
| 3       | **Basic Features of VHDL**  
Major Language Constructs, Lexical Descriptions, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93 |
| 4       | **Basic VHDL Modeling Techniques**  
Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives |
| 5       | **Algorithmic Level Design**  
General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems |
| 6       | **Register Level Design**  
Transition from Algorithmic to Data Flow Descriptions, Timing Analysis |
| 7       | **Gate Level and ASIC Library Modeling**  
Accurate Gate Level Modeling, VITAL: A Standard for the Generation of VHDL Models of Library Elements Error Checking, Configuration Declarations for Gate Level Models, Approaches to Delay Control |
| 8       | **HDL-Based Design Techniques**  
Design of Combinational Logic Circuits, Design of Sequential Logic Circuits |
| 9       | **ASICs and the ASIC Design Process**  
What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis |
| 10      | **Modeling for Synthesis**  
| 12      | **Synthesis Algorithms for Design Automation**  
I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook while I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

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Name (Printed)                      Signature                      Date