2.1 CAD Tool Taxonomy

Legend
S - System  G - Gate
Ch - Chip   CR - Circuit
R - Register L - Layout
2.3 Simulators – Modeling Elements

• A __________ is a major modeling element in VHDL. The correspondence between __________ and ____________ can be ____________, ____________, or ____________.

• Example #1

   ![Digital device diagram](image1)

   ![Graphical representation](image2)

   ![VHDL process](image3)

   ```vhdl
   process(CLK,R)
   begin
     if R='0' then q <= '0';
     elsif CLK'EVENT and CLK='1'
       then Q <= D;
     end if;
   end process;
   ```

• Example #2

   ![Graphical representation](image4)

   • There is also a correspondence between _______ and ___________.
   • A process is activated when a triggering signal ___________. Non-triggering, or ___________, signals do not cause activation and are represented graphically by using an ________________.
   • Signal __________ consist of a ________ and a _________ at which that _________ is scheduled to occur (SN, V). When a value on a signal changes, that is a ________________ (processes are triggered by these).
### 2.4 Simulators – The Simulation System

- The simulation process proceeds as follows:
  - Initialization
  - While there are new time queue entries
    - For each current signal event
    - Trigger the appropriate process
    - Execute activated processes

- Simulator Organization
- Language Scheduling Mechanisms
- Simulation Efficiency
- A complete system consists of
  - Analysis -
  - Elaboration -

### 2.5 Simulation Aids

- Model Preparation
  - Straight textual entry
  - Graphical entry
    - State diagram
    - Flow chart
- Model Test Vector Development
  - Manual
  - Graphical
  - Read from file
  - Macros in simulator
- Model Debugging
  - VHDL analyzers do range checking
  - Graphical debuggers are part of the simulation environment
2.7 Synthesis Tools

- Current tools work primarily at the register level of abstraction

(a) Direct translation to iterative network.

(b) Optimization for 2-input XOR gates at maximum speed.

(c) Maximum speed implementation using 2 and 3 input XOR gates