9.1 What is an ASIC?

- An ASIC is an
  ___________________________________________.
- There is a range of flexibility involved in IC design
  - Full Custom
  - __________________
  - __________________
  - Field Programmable
9.2 ASIC Circuit Technology

**Diagram:**

- **IN** connected to **VDD** and **GND**
- **A** and **B** connected to **GND**
- **OUT** connected to **VDD** and **GND**

- **VIN** connected to **GRD**
- **VOUT** connected to **GRD** and **+5**
9.3 Types of ASICs - PLDs
9.3 Types of ASICs - Field Programmable Gate Arrays
9.3 Types of ASICs - Field Programmable Gate Arrays (CLBs)
9.3 Types of ASICs - FPGA Interconnect

• Switch Technology
  • Reprogrammable
    • _______, _______, _______, _________
  • Programmable Once
    • ______________
9.3 Types of ASICs - FPGA Interconnect Structures

- CLB
- PIP
- Xbar Switch Point
- 4 x 4 Xbar
9.3 Types of ASICs - More on FPGA Interconnect

Routing between CLBs can encounter many delays leading to:

Xilinx - hierarchy of wire types in wire tracks
Actel - three layers of metal using entire chip surface

FPGAs contain special logic for
Input/Output Blocks
Bussed Tristate Systems
Decoders
Oscillators
Fast Adders
RAM
9.3 Types of ASICs - Gate Arrays

- Sea of gates with mask programmable interconnections
- Disadvantage - All transistors are created equal
9.3 Types of ASICs - Standard Cell

Diagram of a standard cell with labels such as m1, n-well, contact, pdiff, metal2, poly, ndiff, p-well, and pdiff.
9.3 Types of ASICs - Standard Cell Layout

All cells are the same ________ but different ________. So, they are put together in ________ with ________ for ________ left between the ________.
9.3 Types of ASICs - Standard Cells

Mixed with Block Compiled Parts

Standard cells work well for ____________ but are inefficient for modules with regular structure such as ____________, ____________, ____________, ____________, ____________ and ____________.

These blocks may be integrated with a standard cell portion of a chip.

These fixed blocks may be IP.
9.3 Types of ASICs - Full Custom Chips

The designer has complete control over the design within the design rules. The main use is analog and mixed-signal designs.
9.3 Types of ASICs - Relative Cost of ASICs and FPGAs

The design approach used depends on
__________
__________

For cost, we must consider _______ costs and _______ costs. _______ costs are incurred independent of volume, _______ costs are incurred per item.

Total product cost = fixed product cost + variable product cost * products sold

<table>
<thead>
<tr>
<th></th>
<th>Fixed</th>
<th>Variable</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>$21,800</td>
<td>$39</td>
</tr>
<tr>
<td>MPG A</td>
<td>$86,000</td>
<td>$10</td>
</tr>
<tr>
<td>CBIC</td>
<td>$146,000</td>
<td>$8</td>
</tr>
</tbody>
</table>
### 9.3 Types of ASICs - Where are the Break-Even Points?

<table>
<thead>
<tr>
<th></th>
<th>Fixed</th>
<th>Variable</th>
</tr>
</thead>
<tbody>
<tr>
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<td>$10</td>
</tr>
<tr>
<td>CBIC</td>
<td>$146,000</td>
<td>$8</td>
</tr>
</tbody>
</table>
9.3 Types of ASICs - Time to Market Impact
9.4 The ASIC Design Process - Overview

- Behavioral Model Development
  - Behavioral Model Validation
  - Logic Synthesis
    - Post Synthesis Logic Simulation
      - System Partitioning
        - Floor Planning
          - Placement
            - Routing
              - Circuit Extraction
                - Post Lay-Out Simulation
                  - ASIC Sell off
9.4 The ASIC Design Process - Standard Cell ASIC Synthesis

This is what we were doing in Synopsys

Steps
  Analyze
  Elaborate
  Compile
  Report
  Save
9.4 The ASIC Design Process - Synthesis Tool Use Strategies

Experiment
Use scripts to control your experimentation

Example

```vhdl
entity SM_COUNT is
  port(CLK, CON, RESET: in std_logic;
       COUNT: inout std_logic_vector(3 downto 0));
end SM_COUNT;
architecture ALG of SM_COUNT is
begin
  process(CLK, CON, RESET)
  begin
    if RESET = '1' then
      COUNT <= "0000";
    elsif CLK'EVENT and CLK='1' then
      if CON = '1' then
        COUNT <= INC(COUNT);
      end if;
    end if;
  end if;
end process;
end ALG;
```

analyze -format vhdl sm_count.vhd
elaborate SM_COUNT -architecture ALG
create_clock -period 10
            -waveform {0 5} CLK
compile
write -format vhdl -output SM_COUNT_1.VHD
write -format ddc
            -output SM_COUNT_1.ddc
report_timing > SM_COUNT_1.rep
report_area >> SM_COUNT_1.rep
9.4 The ASIC Design Process - Timing Report Output from Synthesis

*****************************************************************************
Report : timing  -path full -delay max -max_paths 1
Design : SM_COUNT
Version: Z-2007.03-SP3
Date   : Mon Oct 22 11:24:18 2007
*****************************************************************************
Operating Conditions:  Wire Load Model Mode: top
Startpoint: COUNT_reg[1] (rising edge-triggered flip-flop clocked by CLK)
Endpoint: COUNT_reg[3] (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK  Path Type: max

Point .............................................. Incr Path
----------------------------------------------- -------
clock CLK (rise edge) ........................ 0.00 0.00
clock network delay (ideal) .................. 0.00 0.00
COUNT_reg[1]/CP (FD2) ....................... 0.00 0.00 r
COUNT_reg[1]/Q (FD2) ......................... 1.63 1.63
U9/2 (IV) ....................................... 0.21 1.84 f
U8/2 (NR2) ...................................... 1.33 3.16 r
U6/2 (ND2) ...................................... 0.30 3.46 f
U5/2 (EN) ........................................ 1.13 4.59 f
COUNT_reg[3]/D (FD2) ......................... 0.00 4.59 f
data arrival time ............................ 4.59

clock CLK (rise edge) ........................ 10.00 10.00
clock network delay (ideal) .................. 0.00 10.00
COUNT_reg[3]/CP (FD2) ....................... 0.00 10.00 r
library setup time .......................... -0.85 9.15
data required time ......................... 9.15
-------------------------------------------------------------
data required time .......................... 9.15
data arrival time ................................ -4.59
-------------------------------------------------------------
slack (MET) ..................................... 4.56
9.4 The ASIC Design Process - Area Report Output from Synthesis

*****************************************************************
Report : area
Design : SM_COUNT
*****************************************************************

Library(s) Used: lsi_10k
(File: /apps/synopsys/Z-2007.03 SP3/libraries/syn/lsi_10k.db)
Number of ports:  7
Number of nets:    16
Number of cells:  13
Number of references:  6

Combinational area:  17.000000
Noncombinational area:  36.000000
Net Interconnect area: undefined  (No wire load specified)

Total cell area:  53.000000
Total area:  undefined
9.4 The ASIC Design Process - Minimum Delay Circuits

- Ideal Delay vs. Area Curve

- Realistic Delay vs. Area Curve
9.4 The ASIC Design Process - Setting Timing Constraints

- Once critical paths are identified, they can be used as a target for synthesis performance.
  - `set_max_delay 3 -from "COUNT_reg[1]/CP" -to "COUNT_reg[3]/D"

- To exert maximum effort to minimize the delay along each path
  - `set_max_delay 0 -to all_outputs() + all_registers(-data_pins)`
9.4 The ASIC Design Process - Setting Timing Constraints

```
analyze -format vhdl sm_count.vhd
elaborate SM_COUNT -architecture ALG
create_clock -period 10 -waveform {0 5} CLK
compile
report_timing > SM_COUNT_1.rep
report_area >> SM_COUNT_1.rep
set_max_delay 3 -from "COUNT_reg[1]/CP" -to "COUNT_reg[3]/D"
calculate
report_timing >> SM_COUNT_1.rep
report_area >> SM_COUNT_1.rep
set_max_delay 3 -from "COUNT_reg[1]/CP" -to "COUNT_reg[3]/D"
calculate
report_timing >> SM_COUNT_1.rep
report_area >> SM_COUNT_1.rep
write -format vhdl -output SM_COUNT_1.VHD
write -format ddc -output SM_COUNT_1.ddc
```
9.4 The ASIC Design Process - Setting Timing Constraints

analyze -format vhdl sm_count.vhd
elaborate SM_COUNT -architecture ALG
create_clock -period 10 -waveform {0 5} CLK
set_max_delay 0 -to all_outputs() + all_registers(-data_pins)
compile
report_timing > SM_COUNT_2.rep
report_area >> SM_COUNT_2.rep
set_max_delay 3 -from "COUNT_reg[0]/CP" -to "COUNT_reg[3]/D"
compile
report_timing >> SM_COUNT_2.rep
report_area >> SM_COUNT_2.rep
set_max_delay 3 -from "COUNT_reg[0]/CP" -to "COUNT_reg[3]/D"
compile
report_timing >> SM_COUNT_2.rep
report_area >> SM_COUNT_2.rep
write -format vhdl -output SM_COUNT_2.VHD
write -format ddc -output SM_COUNT_2.ddc
9.4 The ASIC Design Process - Optimally Timed Synchronous Circuits

Possible Paths

- Inputs to Registers \( T_{in} < T_{clk}/2 \)
- Registers to Registers \( T_{int} < T_{clk} \)
- Registers to Outputs \( T_{out} < T_{clk}/2 \)
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
entity ADD is
  port(CLK,RESET: in std_logic; A: in signed(1 downto 0); C: buffer signed(1 downto 0));
end ADD;
architecture ALG of ADD is
begin
  process(CLK)
  begin
    if RESET = '1' then C <= "00";
    elsif CLK'EVENT and CLK = '1' then
      C <= A + C;
    end if;
  end process;
end ALG;
9.4 The ASIC Design Process - Optimal Timing First Attempt

```bash
analyze -format vhdl add.vhd
elaborate ADD -architecture ALG
create_clock -period 10 -waveform {0 5} CLK
compile -map_effort high
report_timing
report_timing -from "A[1]"
```
9.4 The ASIC Design Process - Optimal Timing First Attempt

****************************************
Report: timing -path full  -delay max  -max_paths 1
Design: ADD
Version: 2001.08-SP1
Date   : Thu Mar 18 13:43:44 2004
****************************************
Startpoint: C_reg[1] (rising edge-triggered flip-flop clocked by CLK)
Endpoint: C_reg[1] (rising edge-triggered flip-flop clocked by CLK)

<table>
<thead>
<tr>
<th>Point</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock CLK (rise edge)</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>C_reg[1]/CP (FD2)</td>
<td>0.00</td>
<td>0.00 r</td>
</tr>
<tr>
<td>C_reg[1]/Q (FD2)</td>
<td>1.48</td>
<td>1.48 r</td>
</tr>
<tr>
<td>U20/Z (EN)</td>
<td>1.13</td>
<td>2.61 f</td>
</tr>
<tr>
<td>U19/Z (EO)</td>
<td>1.13</td>
<td>3.73 f</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>0.00</td>
<td>3.73 f</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>3.73</td>
</tr>
<tr>
<td>clock CLK (rise edge)</td>
<td>10.00</td>
<td>10.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
<td>0.00</td>
<td>10.00</td>
</tr>
<tr>
<td>C_reg[1]/CP (FD2)</td>
<td>0.00</td>
<td>10.00 r</td>
</tr>
<tr>
<td>library setup time</td>
<td>-0.85</td>
<td>9.15</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>9.15</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>9.15</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>-3.73</td>
</tr>
<tr>
<td>slack (MET)</td>
<td></td>
<td>5.42</td>
</tr>
</tbody>
</table>
## 9.4 The ASIC Design Process - Optimal Timing First Attempt

Performing report Timing on port 'A[1]'.
Performing report Timing on pin 'C_reg[1]/D'.

```
****************************************
Report : timing -path full -delay max -max_paths 1
Design : ADD
Date   : Thu Mar 18 13:43:44 2004
****************************************
```

Startpoint: A[1] (input port)
Endpoint: C_reg[1] (rising edge-triggered flip-flop clocked by CLK)

<table>
<thead>
<tr>
<th>Point</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock (input port clock) (rise edge)</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>input external delay</td>
<td>0.00</td>
<td>0.00 f</td>
</tr>
<tr>
<td>A[1] (in)</td>
<td>0.00</td>
<td>0.00 f</td>
</tr>
<tr>
<td>U20/Z (EN)</td>
<td>1.13</td>
<td>1.13 f</td>
</tr>
<tr>
<td>U19/Z (EO)</td>
<td>1.13</td>
<td>2.25 f</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>0.00</td>
<td>2.25 f</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>2.25</td>
</tr>
<tr>
<td>clock CLK (rise edge)</td>
<td>10.00</td>
<td>10.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
<td>0.00</td>
<td>10.00</td>
</tr>
<tr>
<td>C_reg[1]/CP (FD2)</td>
<td>0.00</td>
<td>10.00 r</td>
</tr>
<tr>
<td>library setup time</td>
<td>-0.85</td>
<td>9.15</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>9.15</td>
</tr>
<tr>
<td>data required time</td>
<td>9.15</td>
<td></td>
</tr>
<tr>
<td>data arrival time</td>
<td>-2.25</td>
<td></td>
</tr>
<tr>
<td>slack (MET)</td>
<td>6.90</td>
<td></td>
</tr>
</tbody>
</table>
9.4 The ASIC Design Process - Optimal Timing Second Attempt

analyze -format vhdl add.vhd
elaborate ADD -architecture ALG
create_clock -period 10 -waveform {0 5} CLK
compile
set_max_delay 3 -from "C_reg[0]/CP" -to "C_reg[0]/D"
compile
report_timing
report_timing -from "A[1]" -to "C_reg[1]/D"
9.4 The ASIC Design Process - Optimal Timing Second Attempt

*******************************************************************
Report : timing -path full -delay max -max_paths 1
Design : ADD
Version: 2001.08-SP1
Date   : Thu Mar 18 13:44:23 2004
*******************************************************************

Startpoint: C_reg[0] (rising edge-triggered flip-flop clocked by CLK)
Endpoint: C_reg[0] (rising edge-triggered flip-flop clocked by CLK)
Path Group: CLK
Path Type: max

<table>
<thead>
<tr>
<th>Point</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_reg[0]/CP (FD2P)</td>
<td>0.00</td>
<td>0.00  r</td>
</tr>
<tr>
<td>C_reg[0]/Q (FD2P)</td>
<td>1.41</td>
<td>1.41  r</td>
</tr>
<tr>
<td>U26/Z (EOP)</td>
<td>1.09</td>
<td>2.50  f</td>
</tr>
<tr>
<td>C_reg[0]/D (FD2P)</td>
<td>0.00</td>
<td>2.50  f</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>2.50</td>
</tr>
<tr>
<td>max_delay</td>
<td>3.00</td>
<td>3.00</td>
</tr>
<tr>
<td>library setup time</td>
<td>-0.85</td>
<td>2.15</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>2.15</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>2.15</td>
</tr>
<tr>
<td>slack (VIOLATED)</td>
<td></td>
<td>-0.35</td>
</tr>
</tbody>
</table>
### 9.4 The ASIC Design Process - Optimal Timing Second Attempt

Report: timing -path full -delay max -max_paths 1  
Design: ADD  
Version: 2001.08-SP1  
Date: Thu Mar 18 13:44:23 2004

Startpoint: A[1] (input port)  
Endpoint: C_reg[1] (rising edge-triggered flip-flop clocked by CLK)

<table>
<thead>
<tr>
<th>Point</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock (input port clock) (rise edge)</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>input external delay</td>
<td>0.00</td>
<td>0.00 f</td>
</tr>
<tr>
<td>A[1] (in)</td>
<td>0.00</td>
<td>0.00 f</td>
</tr>
<tr>
<td>U28/Z (EO3P)</td>
<td>1.99</td>
<td>1.99 f</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>0.00</td>
<td>1.99 f</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>1.99</td>
</tr>
<tr>
<td>clock CLK (rise edge)</td>
<td>10.00</td>
<td>10.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
<td>0.00</td>
<td>10.00</td>
</tr>
<tr>
<td>C_reg[1]/CP (FD2)</td>
<td>0.00</td>
<td>10.00 r</td>
</tr>
<tr>
<td>library setup time</td>
<td>-0.85</td>
<td>9.15</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>9.15</td>
</tr>
<tr>
<td>data required time</td>
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<td>9.15</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>9.15</td>
</tr>
<tr>
<td>slack (MET)</td>
<td></td>
<td>7.16</td>
</tr>
</tbody>
</table>
9.4 The ASIC Design Process - Optimal Timing Third Attempt

analyze -format vhdl add.vhd
elaborate ADD -architecture ALG
create_clock -period 10 -waveform {0 5} CLK
compile
set_max_delay 2.5 -from "C_reg[0]/CP" -to "C[0]"
compile
report_timing
report_timing -from "A[0]" -to "C_reg[0]/D"
### 9.4 The ASIC Design Process - Optimal Timing Third Attempt

<table>
<thead>
<tr>
<th>Startpoint: C_reg[0] (rising edge-triggered flip-flop clocked by CLK)</th>
<th>Endpoint: C_reg[1] (rising edge-triggered flip-flop clocked by CLK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Point</td>
<td>Incr</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>clock CLK (rise edge)</td>
<td>0.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
<td>0.00</td>
</tr>
<tr>
<td>C_reg[0]/CP (FD2)</td>
<td>0.00</td>
</tr>
<tr>
<td>C_reg[0]/Q (FD2)</td>
<td>1.53</td>
</tr>
<tr>
<td>U24/Z (ND2)</td>
<td>0.78</td>
</tr>
<tr>
<td>U27/Z (EO3P)</td>
<td>1.99</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>0.00</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
</tr>
<tr>
<td>clock CLK (rise edge)</td>
<td>10.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
<td>0.00</td>
</tr>
<tr>
<td>C_reg[1]/CP (FD2)</td>
<td>0.00</td>
</tr>
<tr>
<td>library setup time</td>
<td>-0.85</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
</tr>
<tr>
<td>data required time</td>
<td></td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
</tr>
<tr>
<td>slack (MET)</td>
<td></td>
</tr>
</tbody>
</table>
9.4 The ASIC Design Process - Optimal Timing Third Attempt

Startpoint: C_reg[0] (rising edge-triggered flip-flop clocked by CLK)
Endpoint: C[0] (output port)
Path Group: default
Path Type: max

<table>
<thead>
<tr>
<th>Point</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_reg[0]/CP (FD2)</td>
<td>0.00</td>
<td>0.00 r</td>
</tr>
<tr>
<td>C_reg[0]/Q (FD2)</td>
<td>1.63</td>
<td>1.63 r</td>
</tr>
<tr>
<td>C[0] (out)</td>
<td>0.00</td>
<td>1.63 r</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>1.63</td>
</tr>
<tr>
<td>max_delay</td>
<td>2.50</td>
<td>2.50</td>
</tr>
<tr>
<td>output external delay</td>
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<td>2.50</td>
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<tr>
<td>data required time</td>
<td></td>
<td>2.50</td>
</tr>
<tr>
<td>data required time</td>
<td></td>
<td>2.50</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td>2.50</td>
</tr>
<tr>
<td>slack (MET)</td>
<td></td>
<td>0.87</td>
</tr>
</tbody>
</table>
### 9.4 The ASIC Design Process - Optimal Timing Third Attempt

Performing `report_timing` on port 'A[0]'. Performing `report_timing` on pin 'C_reg[0]/D'.

<table>
<thead>
<tr>
<th>Design</th>
<th>Version</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>2001.08-SP1</td>
<td>Thu Mar 18 13:45:00 2004</td>
</tr>
</tbody>
</table>

**Startpoint:** A[0] (input port)  
**Endpoint:** C_reg[0] (rising edge-triggered flip-flop clocked by CLK)  
**Path Group:** CLK

<table>
<thead>
<tr>
<th>Point</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock (input port clock) (rise edge)</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>input external delay</td>
<td>0.00</td>
<td>0.00 f</td>
</tr>
<tr>
<td>A[0] (in)</td>
<td>0.00</td>
<td>0.00 f</td>
</tr>
<tr>
<td>U26/Z (EO)</td>
<td>1.13</td>
<td>1.13 f</td>
</tr>
<tr>
<td>C_reg[0]/D (FD2)</td>
<td>0.00</td>
<td>1.13 f</td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>clock CLK (rise edge)</td>
<td>10.00</td>
<td>10.00</td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
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</tr>
<tr>
<td>C_reg[0]/CP (FD2)</td>
<td>0.00</td>
<td>10.00 r</td>
</tr>
<tr>
<td>library setup time</td>
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<td>9.15</td>
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<tr>
<td>data required time</td>
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<td>9.15</td>
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</tbody>
</table>

**Slack (MET):** 8.02
9.4 The ASIC Design Process - Optimal Timing with I/O Delays

analyze -format vhdl add.vhd
elaborate ADD -architecture ALG
create_clock -period 5 -waveform {0 2.5} CLK
set_input_delay -clock CLK -max -rise 2.5 "A"
set_input_delay -clock CLK -max -fall 2.5 "A"
set_output_delay -clock CLK -max -rise 2.5 "C"
set_output_delay -clock CLK -max -fall 2.5 "C"
compile
report_timing -path end -delay max -max_paths 40 -nworst 5 > add.rpt
9.4 The ASIC Design Process - I/O Delays Schematic
### 9.4 The ASIC Design Process - I/O Delays Timing Report

```
****************************************
Report : timing  -path end -delay max -nworst 5  -max_paths 40
Design : ADD
Date : Mon Mar 31 09:26:31 2003
****************************************

<table>
<thead>
<tr>
<th>Endpoint</th>
<th>Path Delay</th>
<th>Path Required</th>
<th>Slack</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>4.68 f</td>
<td>4.15</td>
<td>-0.53</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>4.68 f</td>
<td>4.15</td>
<td>-0.53</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>4.50 r</td>
<td>4.15</td>
<td>-0.35</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>4.50 r</td>
<td>4.15</td>
<td>-0.35</td>
</tr>
<tr>
<td>C_reg[1]/D (FD2)</td>
<td>4.50 f</td>
<td>4.15</td>
<td>-0.35</td>
</tr>
<tr>
<td>C_reg[0]/D (FD2)</td>
<td>3.59 f</td>
<td>4.15</td>
<td>0.56</td>
</tr>
<tr>
<td>C_reg[0]/D (FD2)</td>
<td>3.59 f</td>
<td>4.15</td>
<td>0.56</td>
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<tr>
<td>C_reg[0]/D (FD2)</td>
<td>3.41 r</td>
<td>4.15</td>
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<td>3.41 r</td>
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<td>0.74</td>
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<td>C[0] (out)</td>
<td>1.63 r</td>
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<td>0.87</td>
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<tr>
<td>C[0] (out)</td>
<td>1.53 f</td>
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<td>0.97</td>
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<tr>
<td>C[1] (out)</td>
<td>1.37 f</td>
<td>2.50</td>
<td>1.13</td>
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<tr>
<td>C[1] (out)</td>
<td>1.19 r</td>
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<td>1.31</td>
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<tr>
<td>C_reg[0]/D (FD2)</td>
<td>2.72 f</td>
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<td>1.43</td>
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```