Extra Credit Homework

Due April 27, 2009

Take the VHDL model of the washing machine you created for Homework #4 and instantiate it in a SystemVerilog top module that also contains an interface and a testbench. In the testbench, use integer random variables to vary the time it takes for full and empty to become ‘1’ after the state is reached where the state machine is waiting for them. Constrain the random variables to be less than or equal to 10 and greater than or equal to 2. Use the following weights for distributions:

- Time to full:  \((2, 5), (3, 8), (4, 10), (5, 15), (6, 15), (7, 15), (8, 15), (9, 10), (10, 7)\)
- Time to empty:  \((2, 5), (3, 5), (4, 8), (5, 15), (6, 15), (7, 20), (8, 20), (9, 7), (10, 5)\)

Run 50 different test cases for your testbench.

Turn in your VHDL and SystemVerilog source files.