The University of Alabama in Huntsville
Electrical and Computer Engineering
Course Syllabus
CPE 426/526 01
Spring 2009


Web Page: http://www.ece.uah.edu/courses/cpe526

Instructor: Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573, email: gaede@ece.uah.edu

Office Hours: T 10 AM – 12 PM, R 3 PM – 4 PM, or by appointment

Grading:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Homework</td>
<td>20 %</td>
</tr>
<tr>
<td>Project</td>
<td>30 %</td>
</tr>
<tr>
<td>Midterm</td>
<td>25 %</td>
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<tr>
<td>Final Exam</td>
<td>25 %</td>
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Graduate Students will have extra and/or different problems on their tests. The grading for the project will be 1/3 for the project presentation and 2/3 for the project report.

Homework: Homework will be submitted and graded electronically. It is due by 11:59 PM on the date it is due. NO late homework will be accepted without extenuating circumstances. Contact me as soon as a problem occurs.

Important Dates:
January 9 – Last day to add a class
January 16 – Last day to withdraw with refund
January 19 – Holiday
January 26 – Last day to apply for Pass/Fail
February 2 – Last day to change from credit to audit
March 16-21 – Spring Break
March 23 – Last day to withdraw
April 6 –Registration for Summer 2009 begins
April 20 – Last MW class

Final Exam: Monday, April 27, 11:30 AM – 2:00 PM

Miscellaneous: Homework will be done individually.
Projects will be done in groups.
Mute your cell phones before you bring them to class.
### Course Outline:

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Topics</th>
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| **1**   | **Structured Design Concepts**  
| **2**   | **Design Tools**  
CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools |
| **3**   | **Basic Features of VHDL**  
Major Language Constructs, Lexical Descriptions, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93 |
| **4**   | **Basic VHDL Modeling Techniques**  
Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives |
| **7**   | **Gate Level and ASIC Library Modeling**  
Accurate Gate Level Modeling, VITAL: A Standard for the Generation of VHDL Models of Library Elements Error Checking, Configuration Declarations for Gate Level Models, Approaches to Delay Control |
| **8**   | **HDL-Based Design Techniques**  
Design of Combinational Logic Circuits, Design of Sequential Logic Circuits |
| **9**   | **ASICs and the ASIC Design Process**  
What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis |
| **10**  | **Modeling for Synthesis**  

Functional Verification Using SystemVerilog
I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook while I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

__________________________  _________________________  _________________
Name (Printed)              Signature                      Date