Consider the combinational logic circuit below. How many possible single stuck-at faults does this circuit have? How many possible multiple stuck-at faults does this circuit have? How many collapsed single stuck-at faults does this circuit have?

There are 14 nodes in the circuit. Thus, there are $14 \times 2 = 28$ single stuck-at faults.

For multiple stuck-at fault, it has $(2 + 1)^{14} - 1 = 4782968$ multiple stuck-at faults.

For collapsed single stuck-at fault:

Number of collapsed faults = $2 \times (\text{number of POs} + \text{number of fanout stems}) + \text{total number of gate (including inverter) inputs} - \text{total number of inverters}$

Here number of POs = 1, number of fanout stems = 3, total number of gate inputs = 10, number of inverter = 2. Therefore, the number of collapsed faults = $2 \times (1 + 3) + 10 - 2 = 16$.

Generate a minimum set of test vectors to completely test an n-input NAND gate under the single stuck-at fault model. How many test vectors are needed?

To detect all single stuck-at faults of the n-input NAND, we need $n+1$ test vectors. In fact, in order to detect the s-a-1 fault at the inputs, the following patterns are needed:

$(01111\ldots1), (10111\ldots1), (11011\ldots1), (11101\ldots1), (11110\ldots1), \ldots, (11111\ldots0)$

In addition, $(1111\ldots1)$ is required to detect s-a-0 faults and the output s-a-1 fault.

The number of failures in $10^9$ hours is a unit (abbreviated FITS) that is often used in reliability calculations. Calculate the MTBF for a system with 500 components where each component has a failure rate of 1000 FITS.

$\lambda = \sum_{i=1}^{k} \lambda_i$, \hspace{1em} $\lambda = \frac{1000}{10^9}$. Thus, $\lambda = 10^{-6} \times 500 = 5 \times 10^{-4}$

$\text{MTBF} = \frac{1}{\lambda} = 2 \times 10^3 = 2000$ hours.
2.1 Calculate the SCOAP controllability and observability measures for a three-input XOR gate and for its NAND-NOR implementation.

2.2 Use the rules given in Tables 2.3 and 2.4 to calculate the probability-based testability measures for a three-input XNOR gate and for its NAND-NOR implementation. Assume that the probability-based controllability values at all primary inputs and the probability-based observability values at all the primary outputs are 0.5 and 1, respectively.
2.4 Calculate the combinational observability of input $a_i$ at output $s_k$, denoted by $O(a_i, s_k)$, where $k > i$, for the $n$-bit ripple-carry adder shown.

\[ s_i = c_i + a_i + b_i , \quad c_{i+1} = c_i(a_i + b_i) + a_i b_i \]

\[ O(a_i, s_i) = O(b_i, s_i) = O(c_i, s_i) = O(s_i), \quad i = 0, \ldots, n - 1. \]

\[ O(a_i, s_k) = \left[ C_1(c_i \oplus b_i) \times \prod_{j=i+1}^{k-1} C_1(a_j \oplus b_j) \right] O(s_k), \quad i = 0, \ldots, n - 1. \]