# MSP430F13x/14x/14x1 Device Erratasheet

## Current Version

### Devices

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<th>WDG2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSP430F133</td>
<td>Q</td>
<td>✓</td>
<td>✓</td>
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<td>MSP430F135</td>
<td>N</td>
<td>✓</td>
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<td>MSP430F147</td>
<td>N</td>
<td>✓</td>
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<td>MSP430F1471</td>
<td>N</td>
<td>✓</td>
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<td>MSP430F148</td>
<td>Q</td>
<td>✓</td>
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<td>MSP430F1481</td>
<td>Q</td>
<td>✓</td>
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<td>MSP430F149</td>
<td>N</td>
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<tr>
<td>MSP430F1491</td>
<td>Q</td>
<td>✓</td>
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<td>✓</td>
<td>✓</td>
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Note: See Appendix for prior revisions

### Package Markings

**PM64: LQFP(PM) 64-pin**

- **YM**: Year and Month Date Code
- **LLL**: LOT Trace Code
- **S**: Assembly Site Code
- **#**: DIE Revision
- **o**: PIN 1

![Package Marking](image)

**PAG64: TQFP(PAG) 64-pin**

- **YM**: Year and Month Date Code
- **LLL**: LOT Trace Code
- **S**: Assembly Site Code
- **#**: DIE Revision
- **o**: PIN 1

![Package Marking](image)

**RTD64: QFN(RTD) 64-pin**

- **YM**: Year and Month Date Code
- **LLL**: LOT Trace Code
- **S**: Assembly Site Code
- **#**: DIE Revision
- **o**: PIN 1

![Package Marking](image)
MSP430F13x/14x/14x1
SLAZ017 – MAY 2005

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<thead>
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<th>Code</th>
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<tbody>
<tr>
<td>TI</td>
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<tr>
<td>YM</td>
<td>Year and Month Date Code</td>
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<tr>
<td>LLLL</td>
<td>LOT Trace Code</td>
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<tr>
<td>S</td>
<td>Assembly Site Code</td>
</tr>
<tr>
<td>#</td>
<td>DIE Revision</td>
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<td>PIN 1</td>
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</tbody>
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Detailed Bug Description

ADC1  ADC1 - Bug description:

Module: ADC12, Function: Start of conversion

In single conversion/sequence mode (CONSEQ=0/1) the next conversion can be started with ADC12SC. It is not required to clear ENC before setting ADC12SC. This is opposite to the specification.

Workaround:
None

ADC5  ADC5 - Bug description:

Module: ADC12, Function: Interrupt flag register

ADC12 interrupt flag may not be set when the CPU simultaneously accesses the ADC12IFG register.

Workaround:
There is no need to access the interrupt flag register to process interrupt situations. Please use the ADC12IV register to identify the interrupt event. The corresponding flag bits will be reset automatically. Additional details are discussed in the device family User's Guide.

ADC7  ADC7 - Bug description:

Module: ADC12, Function: Conversion Time Overflow

The timing overflow flag is set when in sequence mode (CONSEQ=1 or 3) and MSC=0, even if no overflow has occurred.

Workaround:
Verify correct timing and do not enable Conversion-Time Overflow interrupt.

ADC8  ADC8 - Bug description:

Module: ADC12, Function: Interrupt flag register

Clearing flags in the interrupt flag register with a CPU instruction will not clear the latest interrupt flag.

Workaround:
Clear interrupt flags by accessing the conversion-memory registers.
Detailed Bug Description (continued)

ADC9  ADC9 - Bug description:

Module: ADC12, Function: Interrupt vector register

If the ADC12 uses a different clock than the CPU (MCLK) and more than one ADC interrupt is enabled, the ADC12IV register content may be unpredictable for one clock cycle. This will happen, if during the execution of an ADC interrupt another ADC interrupt with higher priority occurs.

Workaround:
- read out ADC12IV twice and use only when values are equal
- use ADC12IFG to determine which interrupt has occurred

ADC10 ADC10 - Bug description:

Module: ADC12: Function: Unintended start of conversion

Accessing ADC12OVIE or ADC12TOVIE at the end of an ADC12 conversion with BIS/BIC commands can cause the ADC12SC bit to be set again right after it was cleared. This might start another conversion if ADC12SC is configured to trigger the ADC (SHS = 0).

Workaround:
If ADC12SC is configured to trigger the ADC, the control bits ADC12OVIE and ADC12TOVIE should only be modified when the ADC is not busy (ADC12BUSY = 0).

BSL3  BSL3 - Bug description:

Module: Bootstrap Loader

Receiving frames with a checksum value equal to a legal address can change the content of this address or the bootstrap loader may stop operation.

Workaround:
Software workaround available.

BSL4  BSL4 - Bug description:

Module: Bootstrap Loader - Flash memory can not be programmed

The bootstrap loader SW cannot program the flash memory.

Workaround:
Software workaround available.
Detailed Bug Description (continued)

**BSL5**

**BSL5 - Bug description:**

Module: Bootstrap Loader

If the RST/NMI pin is configured to NMI the bootstrap loader may not be started. Unpredictable operations will result.

Workaround:
None

**CPU4**

**CPU4 - Bug description:**

Module: CPU, Function PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The Assembler version 1.08 and higher produces correct code. The number of clock cycles is different:

- PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
- PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.
No fix planned.

**FLASH13**

**FLASH13 - Bug description:**

Module: Flash, Function Mass Erase

A mass erase time of >200ms is required. This is not covered by the flash controller.

Workaround possible by executing multiple mass erase cycles.

**PORT3**

**PORT3 - Bug description:**

Module: PORT1/2, Function Port interrupts can get lost

Port interrupts can get lost if they occur during CPU access of the P1IFG and P2IFG registers.

Workaround:
None
Detailed Bug Description (continued)

RES3  
RES3 - Bug description:
Module: General, Function reset

When RST/NMI is held low during power up Vcc, some internal drivers are not reset correctly. This may result in a high Icc current until the internal power-on signal has generated one clock cycle to reset the internal drivers. This limits the time when the access current can occur to the time the power up circuit is active.

Workaround:
None

RES4  
RES4 - Bug description:
Module: General, Reset, No reset if external resistor exceeds certain value

No reset of the device is performed if the external pull down resistor on RST/NMI pin is above a certain limit. The limits are:

- VCC=1.8V: maximum pull down resistor = 12kohm
- VCC=3.0V: maximum pull down resistor = 5kohm
- VCC=3.6V: maximum pull down resistor = 2.5kohm

In addition, a higher current consumption occurs during high/low RST/NMI signal transition when using improper resistors.

Workaround:
Use external resistors below the mentioned values.

TA12  
TA12 - Bug description (same as TB2):
Module: TimerA, Interrupt is lost (slow ACLK)

TimerA counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerA counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerA counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.
Detailed Bug Description (continued)

**TA13**

**TA13 - Bug description:**

Module: TimerA, Unintended modification of OUTx signal

If TimerA is used with an asynchronous clock to MCLK, the PWM output can be disturbed during a modification of the CCTLx register bit OMOD[2] of the corresponding CCRx.

**Workaround:**
Disable TimerA clock or use the same clock source for TimerA and MCLK.

**TB 1**

**TB1 - Bug description:**

Module: TimerB, Function "equal mode" when grouping compare latches

The "equal mode" for loading the compare latches (CLLD=3) cannot be used when compare latches are grouped (TBCLGRP>0).

**No workaround possible.**

**TB2**

**TB2 - Bug description (same as TA12):**

Module: TimerB, Interrupt is lost (slow ACLK)

TimerB counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).

Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerB counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerB counter increment (if TBR = CCRx + 1). This interrupt gets lost.

**Workaround:**
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.
Detailed Bug Description (continued)

TB3 - Bug description:

Module: TimerB, Port is switched to tristate independent of selected function

Incorrect tristate function of Ports P4.0/TB0 ... P4.6/TB6 (TBoutHiZ control). If TBoutHiZ is set to 'high' all ports P4.0/TB0 ... P4.6/TB6 are set to tristate independent of the P4SEL.x control signals. This means a port P4.x is switched to tristate with TBoutHiZ even if it is not selected for TimerB function.

In addition the ports P4.0/TB0 ... P4.6/TB6 are switched to tristate with TBoutHiZ even if the port direction (direction control from module) is set to input. This is in accordance with the spec description, but nevertheless is an unexpected behavior.

No workaround.

Port function as specified:

port P4, P4.0 to P4.6, input/output with Schmitt-trigger

![Diagram of port P4, P4.0 to P4.6, input/output with Schmitt-trigger](image)

x: bit identifier, 0 to 6 for Port P4
Detailed Bug Description (continued)

**Port realization with TB3 bug:**

![Port Diagram]

**TB4**

TB4 - Bug description:

Module: TimerB, group function

If the shadow registers are organized in groups (SHR=1,2 or 3) one shadow register is not loaded correctly. This happens, when the last CCRx register within a group is loaded exactly at the same time as the timer counter reaches the event for loading the shadow registers (TBR=0 or TBR=CCR0).

Workaround:
Ensure that all CCRx-registers within a group are loaded before the shadow register load event occurs.

**TB13**

TB13 - Bug description:

Module: TimerB, Unintended modification of OUTx signal

If TimerB is used with an asynchronous clock to MCLK, the PWM output can be disturbed during a modification of the CCTLx register bit OMOD[2] of the corresponding CCRx.

Workaround:
Disable TimerB clock or use the same clock source for TimerB and MCLK.
Detailed Bug Description (continued)

TB14  TB14 - Bug description:

Module: TimerB, PWM output

The PWM output unit may behave erroneously if the condition for changing the
PWM output (EQUx or EQU0) and the condition for loading the shadow register
TBCLx happens at the same time. Depending on the load condition for the shadow
registers (CLLD bits in TBCCTLx) there are four different possible error conditions:

1. Change CCRx register from any value to CCRx=0
   (e.g. sequence for CCRx = 4 3 2 0 0 0)
2. Change CCRx register from CCRx=0 to any value
   (e.g. sequence for CCRx = 0 0 2 3 4)
3. Change CCRx register from any value to current SHD0 (CCR0) value
   (e.g. sequence for CCRx = 4 2 5 SHD0 3 8)
4. Change CCRx register from current SHD0 (CCR0) value to any value
   (e.g. sequence for CCRx = 4 2 SHD0 5 3 8)

SW workaround:
No general workaround available.

TB15  TB15 - Bug description:

Module: TimerB3, 'Grouping Compare Latch' modes with TBCLx=2 or 3 are not useable

For TimerB3, 'Grouping Compare Latch' modes with control bits
TBCLx=10 or 11 (Bits 14, 13 in TBCTL register) are not useable.
If one of these settings are used, no load of any Compare Latch
TBCLx will happen.

Workaround:
None (Use only TBCLx = 00 or 01 for reliable module operation.)

US13  US13 - Bug description:

Module: USART0, USART1, Function: Unpredictable program execution

USART interrupts requested by URXS can result in unpredictable
program execution if this request is not served within two bit
times of the received data.

Workaround:
Ensure that the interrupt service routine is entered within two bit
times of the received data.
Detailed Bug Description (continued)

US15  US15 - Bug description:
Module: USART0, USART1, Function: UART receive with two stop bits

USART hardware does not detect a missing second stop bit when \( SPB = 1 \). The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround:
None (Configure USART for a single stop bit, \( SPB = 0 \))

WDG2  WDG2 - Bug description:

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:
None
## Appendix: Prior Versions

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</thead>
<tbody>
<tr>
<td>MSP430F133</td>
<td>Q</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>MSP430F135</td>
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<td>✓</td>
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<td>MSP430F147</td>
<td>O</td>
<td>✓</td>
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<td>MSP430F148</td>
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Detailed Bug Description

**ADC11**

ADC11 - Bug description:

Module: ADC12, Function: Temporary leakage current after conversion

The ADC12 causes temporary leakage current after a completed conversion. Duration and magnitude of the leakage current depends on parasitic effects.

Workaround:
None
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