CPE 323 Introduction to Embedded Computer Systems: Introduction

Instructor: Dr. Aleksandar Milenkovic
Lecture Notes

CPE 323

- Syllabus
  - textbook & other references
  - grading policy
  - important dates
  - course outline
- Prerequisites
  - memory organization
  - decoding
  - combinatorial and sequential logic
  - important for system architecture
- Microcomputer Lab (EB 106)
  - Introduction sessions
  - Lab instructor

CPE 323 LAB Session
- on-line LAB manual
- Access cards
- Accounts
- Lab Assistant: Joel Wilder
- Lab sessions
  - #1 - Mon: 5:30 - 7:00pm
  - #2 - Tues: 5:30 - 7:00pm
  - Backup - Tues: 7:00 - 8:30pm
- Sign-up sheet - if needed

Outline

- Embedded systems: structure and organization
- Applications
- Technology Trends
- Historical perspective
Embedded Computer Systems

- Stand alone system based on a microprocessor
- An embedded system – dedicated to a specific application
  - control system/monitoring system
  - optimization for a single function (system resources, extension, ...)
  - block diagram
  - inputs $\rightarrow$ processing $\rightarrow$ outputs
- Number of microprocessors in our environment?

A Microcontroller-Based System

Wireless Body Area Network

Data Flow
Microcomputer Block Diagram

Microprocessor System Architecture

- System Architecture
  - Single Board Computers (SBC)
  - block diagram (modules, cards)
- System bus
  - Multibus, VME, ISA, PCI, ...
  - Multiple masters
- CPU
  - Clock and CPU Control Circuits
    - 1 MHz - 1 GHz
    - power-up and reset circuits
  - Address Decoder
  - Address and Data Bus Buffers
  - Bus Arbitration Control
  - Memory management

Microprocessor System Architecture

- Memory Module
  - Virtual memory / Physical memory
  - ROM, RAM, video memory
  - static/dynamic
- Peripheral Module
  - serial interface
    - RS232 (CRT, mouse), USB, Firewire (IEEE 1394)
  - parallel interface
    - printer interface
  - timer
    - time/frequency measurement

PC architecture
Von Neumann Architecture
- Processing Elements
  - sequential execution
- Read/Write Memory
  - linear array of fixed size cells
- I/O unit
- Address/Data/Control bus

Von Neumann Architecture

Von Neumann vs. Harvard

Block Diagram of a Personal Computer
A Typical Small Embedded System – Digital Thermometer

A Microcontroller-Based System

Computing History

PlayStation Portable (PSP)
- Approx. 170 mm (L) x 74 mm (W) x 23 mm (D)
- Weight: Approx. 260 g (including battery)
- CPU: PSP CPU (clock frequency 1~333MHz)
- Main Memory: 32MB
- Embedded DRAM: 4MB
- Profile: PSP Game, UMD Audio, UMD Video

Eniac, 1946
- (first stored-program computer)
- Occupied 50x30 foot room,
- weighted 30 tonnes,
- contained 18000 electronic valves,
- consumed 25KW of electrical power;
- capable to perform 100K calc. per second

Understanding computers ....

- User perspective
  - Applications: What do we do with them?
  - Price: How much do they cost?
    - To purchase and to operate
  - Convenience: How difficult is to use them?

- Designer perspective
  - Size: How large are they? (UP)
  - Speed: How many operations ...? (UP)
  - Power: What is energy consumed? (UP)
  - Complexity: How complex are they to build?
Evaluate Existing Systems for Bottlenecks
Simulate New Designs and Organizations
Implement Next-Generation System

Evaluate Existing Systems for Bottlenecks
Simulate New Designs and Organizations
Implement Next-Generation System

Intel: First 30+ Years

- Intel 4004
  - November 15, 1971
  - 4-bit ALU, 108 KHz, 2,300 transistors, 10-micron technology
- Intel Pentium 4
  - August 27, 2001
  - 32-bit architecture, 1.4 GHz (now 3.08), 42M transistors (now 55+M), 0.18-micron technology (now 0.09)

Technology Directions: SIA Roadmap

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size (nm)</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>Logic trans/cm²</td>
<td>6.2M</td>
<td>18M</td>
<td>36M</td>
<td>64M</td>
<td>180M</td>
<td>300M</td>
</tr>
<tr>
<td>Cost/trans (mc)</td>
<td>1.735</td>
<td>2.90</td>
<td>3.95</td>
<td>5.60</td>
<td>9.09</td>
<td>122</td>
</tr>
<tr>
<td>Pads/chip</td>
<td>1867</td>
<td>2553</td>
<td>3492</td>
<td>4776</td>
<td>6532</td>
<td>8935</td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>1250</td>
<td>2100</td>
<td>3500</td>
<td>6000</td>
<td>10000</td>
<td>16900</td>
</tr>
<tr>
<td>Chip size (mm²)</td>
<td>340</td>
<td>430</td>
<td>520</td>
<td>620</td>
<td>750</td>
<td>900</td>
</tr>
<tr>
<td>Wiring levels</td>
<td>6-7</td>
<td>7-8</td>
<td>8-9</td>
<td>9</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Power supply (V)</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>0.9</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>High-perf pow (W)</td>
<td>90</td>
<td>130</td>
<td>160</td>
<td>170</td>
<td>175</td>
<td>183</td>
</tr>
</tbody>
</table>

Trends & Challenges

- Processor/memory discrepancy
- Memory hierarchy
- On-chip/off-chip memory
- Microprocessor execution
- Fetch > Decode > Execute
- System on a chip - Microcontroller
- Cost, smaller PCB, reliability, power.
- Applications
- Evolution
  - Microprocessor
  - Microprocessor-on-a-chip
  - System-on-a-chip
  - Distributed-system-on-a-chip
More on Challenges

- Scalability
  - billions of small devices
  - performance
- Availability
  - hardware changes
  - system upgrade
  - failures
  - code enhancements
- Fault tolerance

Performance Trends

<table>
<thead>
<tr>
<th>Year</th>
<th>Proc.</th>
<th>MIPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1969</td>
<td>4004</td>
<td>0.06</td>
</tr>
<tr>
<td>1970's 808x</td>
<td>0.64</td>
<td></td>
</tr>
<tr>
<td>1982</td>
<td>286</td>
<td>1</td>
</tr>
<tr>
<td>1985</td>
<td>386</td>
<td>5</td>
</tr>
<tr>
<td>1989</td>
<td>486</td>
<td>20</td>
</tr>
<tr>
<td>1993</td>
<td>Pentium</td>
<td>100</td>
</tr>
<tr>
<td>1996</td>
<td>P II</td>
<td>250</td>
</tr>
<tr>
<td>1999</td>
<td>P III</td>
<td>500</td>
</tr>
<tr>
<td>2000</td>
<td>P 4</td>
<td>1500</td>
</tr>
</tbody>
</table>

Clock Frequency Growth Rate

- 30% per year
Transistor Count Growth Rate

Moore's Law

Transistor Count Growth Rate

General Technology Trends
- Microprocessor performance increases 50%-100% per year
- Transistor count doubles every 3 years
- DRAM size quadruples every 3 years
- Huge investment per generation is carried by huge commodity market

Storage
- Divergence between memory capacity and speed more pronounced
  - Capacity increased by 100x from 1980-95, speed only 2x
  - Gigabit DRAM by c. 2000, but gap with processor speed much greater
  - Larger memories are slower, while processors get faster
  - Need to transfer more data in parallel
  - Need deeper cache hierarchies
  - How to organize caches?

Instruction Sets
- Software costs growing faster than hardware costs (1970s)
  - Machine language v.s. HLL
  - Support for high-level languages
  - Gap between high level languages and computer hardware - semantic gap
- CISC - Complex Instruction Set Architecture
  - Variety of instructions and addressing modes
  - DEC VAX
- HLLCA - High Level Language Computer Architecture
RISC Architectures

- Resolve problems using simpler architecture
  - "The case for the reduced instruction set computers" Patterson & Ditzel [1980]
- Stanford MIPS (Hennessy, 1981)
- Commercial processors: MIPS R2000 (1986), IBM RS6000, SPARC, PowerPC, etc.
- Good design methodology
- Efficient pipelining and compiler-assisted scheduling of pipeline
- Make the Common Case Fast
  - favor the frequent case

Program Execution Time

\[ T = \sum_i n_i \cdot CPI_i \cdot T_{\text{cycle}} \]

For all instructions in the instruction set

- processor cycle time [s]
- cycles per instruction
- instruction count

80x86 Instruction Mix for SPECint92 Programs [PatHen96]

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>load</td>
<td>22%</td>
</tr>
<tr>
<td>cond. branch</td>
<td>20%</td>
</tr>
<tr>
<td>compare</td>
<td>16%</td>
</tr>
<tr>
<td>store</td>
<td>12%</td>
</tr>
<tr>
<td>add</td>
<td>8%</td>
</tr>
<tr>
<td>and</td>
<td>6%</td>
</tr>
<tr>
<td>sub</td>
<td>5%</td>
</tr>
<tr>
<td>mov reg-reg</td>
<td>4%</td>
</tr>
<tr>
<td>or</td>
<td>1%</td>
</tr>
<tr>
<td>xor, not, etc.</td>
<td>1%</td>
</tr>
<tr>
<td>uncond. branch</td>
<td>1%</td>
</tr>
<tr>
<td>call</td>
<td>1%</td>
</tr>
<tr>
<td>return, jmp indirect</td>
<td>1%</td>
</tr>
<tr>
<td>shift</td>
<td>1%</td>
</tr>
</tbody>
</table>

80x86 Instruction Execution

A=B+C
result = op1 OPERATION op2
ADD R1, M(1000)

<table>
<thead>
<tr>
<th>Stage</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td>100ns</td>
</tr>
<tr>
<td>ID</td>
<td>100ns</td>
</tr>
<tr>
<td>OF</td>
<td></td>
</tr>
<tr>
<td>EX</td>
<td>1ns</td>
</tr>
<tr>
<td>ST</td>
<td>1ns</td>
</tr>
<tr>
<td>IF</td>
<td></td>
</tr>
</tbody>
</table>

When \( f = 5\text{MHz} \) \((70s)\)
- \( T_{\text{cycle}} = 200\text{ns} \)
- \( T_{\text{mem}} = 200\text{ns} \)

When \( f = 1000\text{MHz} \) \((90s)\)
- \( T_{\text{cycle}} = 1\text{ns} \)
- \( T_{\text{mem}} = 50\text{ns} \)

3 × 100ns = 300ns
2 × 1ns = 2ns
302ns
Pipeline

CPI = 1

program

#1

#2

#3

#4

#5

if( ) ...

CPI = 1

INSTR

#1

#2

#4

#5

#100

CPU/EE 421/521 Microcomputers