Homework #4: CPE/EE 421/521

1. (15 points) Bus cycles, performance, power

A. (5 points) How many (if any) wait states must be inserted for the following CPU and memory parameters:
   - M68000 CPU operates at 12.5 MHz,
   - data setup time $t_{DICL}$ is 10ns,
   - clock low to address valid $t_{CLAV}$ is 55ns,
   - and the memory access time $t_{A}$ is 450ns.

B. (5 points) Compare performance of two platforms PA and PB assuming the following. For a set of relevant benchmarks, the total number of instructions executed is $N_A$ and $N_B$, respectively; $N_A = 1.8 \times N_B$. Clock frequency of platform A if $F_A = 1.2 \times F_B$, CPI$_A = 4$ and CPI$_B = 8$ (CPI – Cycles per Instruction). Which one would you select assuming that they have the same price?

C. (5 points) We are considering energy efficiency of a computational task for two configurations of a wireless intelligent sensor. The computation is performed 5 times per second (system frequency is 5Hz) and one execution takes 124,800 processor clock cycles.
   - Configuration C1: processor clock frequency is 8MHz, power supply is 3.3V;
   - Configuration C2: processor clock frequency is 5MHz, power supply is 2.4V.
   Ignoring energy consumed when the processor is inactive which configuration is more energy efficient and how many times ($E_{C1}/E_{C2} = ?$)?
2. (15 points) Exceptions
A. (5 points) What are autovectored interrupts. Explain. How does M68000 recognize this type of interrupts?

B. (5 points) Illustrate the flowchart for an interrupt acknowledge sequence.

Processor

Interrupting Device

C. (5 points) List at least 5 software (internal) exceptions implemented in the M68000.

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3. (70 points) CPU Hardware Model

Design microcomputer system with the MC68000 microprocessor with the following characteristics.

- Supervisor program memory of 128KB is implemented using 64K×4 EPROM components, starting at the address $00 0000. 64K×4 EPROM components require 2 wait cycles for bus read cycles. Control inputs for 64Kx4 EPROM components are CE* and OE*.
- Supervisor data memory of 32KB is implemented using RAM 8K×8bit components and resides in the consecutive address window. RAM 8K×8bit components require no wait cycles for write, and one wait cycle for read. Control inputs for RAM 8K×8bit components are CE*, OE*, and WE.
- User program and data memory of 64KB is implemented using 16K×8bit RAM components and resides at the address $10 0000. RAM 16K×8bit components require no wait cycles for write, and one wait cycle for read. Control inputs for RAM 16K×8bit components are CE*, OE*, and WE.
- Two 8-bit peripherals (PER2 and PER3) using 32-byte address windows starting at address $20 0000. Both peripherals require 1 wait cycle for read, write, and IACK cycles. Interrupt mechanism is vectored. PER2 is connected to IRQ2 and PER3 to IRQ3. Control inputs for the peripherals are CE*, IRQ*, IACK,* and WE.

Your solution should include: processor with all relevant lines, memory subsystem, i/o subsystem, corresponding interrupt interface, and decoding logic.

You may use AND, OR, NOT, NAND, NOR, XOR logic gates, LS138 (3 to 8 decoder), LS148 (priority encoder) or any other standard digital circuits.

Bonus question:
Add necessary logic that will allow the microcomputer system to recover from an irregular bus cycle (DTACK* is not generated).