CPE/EE 421
Microcomputers
Instructor: Dr Aleksandar Milenkovic
Lecture Notes
S01

*Material used is in part developed by
Dr. D. Raskovic and Dr. E. Jovanov

CPE/EE 421 Microcomputers

➢ Syllabus
  ❖ textbook & other references
  ❖ grading policy
  ❖ important dates
  ❖ course outline

➢ Prerequisites
  ❖ memory organization
  ❖ decoding
  ❖ combinatorial and sequential logic
  ❖ important for system architecture

➢ Microcomputer Lab (EB 106)
  ❖ Introduction sessions
  ❖ Lab instructor
CPE/EE 421 Microcomputers

- LAB Session
  - on-line LAB manual
  - Access cards
  - Accounts
- Lab Assistant: Joel Wilder
- Lab sessions
  - Lab session #1: Monday 6:00 – 8:00 PM
  - Lab session #2: Monday 8:00 – 10:00 PM
- Sign-up sheet - if needed

Microcomputer

- Stand alone system
  based on a microprocessor
- An embedded system –
dedicated to a specific application
  - control system/monitoring system
  - optimization for a single function
    (system resources, extension, …)
  - block diagram
    - inputs → processing → outputs
- Number of microprocessors
  in our environment?
Microprocessor System Architecture

- System Architecture
  - Single Board Computers (SBC)
  - block diagram (modules, cards)
- System bus
  - Multibus, VME, ISA, PCI, ...
  - Multiple masters
- CPU
  - Clock and CPU Control Circuits
    - 1 MHz - 1 GHz
    - power-up and reset circuits
  - Address Decoder
  - Address and Data Bus Buffers
  - Bus Arbitration Control
  - Memory management

Microprocessor System Architecture #2

- Memory Module
  - Virtual memory / Physical memory
  - ROM, RAM, video memory
  - static/dynamic
- Peripheral Module
  - serial interface
    - RS232 (CRT, mouse), USB, Firewire (IEEE 1394)
  - parallel interface
    - printer interface
  - timer
    - time/frequency measurement
Microprocessor System Architecture #3

- PC architecture

![Block Diagram of a personal computer](image)
A Typical Small Embedded System – Digital Thermometer

A Microcontroller-Based System
A Microcontroller-Based System

Wireless Body Area Network

- LCD
- RS232
- RS232 controller
- Analog I/O
- 2-axes joystick
- LEDs
- Switches
- Thermistor
- Keypad
- Keypad

Wireless Body Area Network

- ECG & tilt sensor
- PPG & movement sensor
- Wireless gateway & temperature/humidity sensor

Body Area Network

Movement sensors

ZigBee or custom wireless

GPRS

Internet

Personal Server

Emergency Server

Medical Server (Mayo Clinic)

Physician’s Server
Conventional Computer Architecture

Von Neumann Architecture

memory

W bits

0
1
2
3
N
log₂N

Read/Write Memory

PE
(Processing Element)

Control Unit

ALU

I/O
(peripherals)

address
control
data

Microprocessors - History

- Implementations
  - size (room, cabinet, desktop, handheld, ...)
  - speed (doubling 18-20 months)
  - power consumption

- Von Neumann Architecture
  - Processing Elements
    - sequential execution
  - Read/Write Memory
    - linear array of fixed size cells
    - Data and instruction store
  - I/O unit
  - Address/Data/Control bus
Intel: First 30+ Years

- **Intel 4004**
  - November 15, 1971
  - 4-bit ALU, 108 KHz, 2,300 transistors, 10-micron technology

- **Intel Pentium 4**
  - August 27, 2001
  - 32-bit architecture, 1.4 GHz (now 3.08), 42M transistors (now 55+M), 0.18-micron technology (now 0.09)

Technology Directions: SIA Roadmap

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size (nm)</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>Logic trans/cm²</td>
<td>6.2M</td>
<td>18M</td>
<td>39M</td>
<td>84M</td>
<td>180M</td>
<td>390M</td>
</tr>
<tr>
<td>Cost/trans (mc)</td>
<td>1.735</td>
<td>.580</td>
<td>.255</td>
<td>.110</td>
<td>.049</td>
<td>.022</td>
</tr>
<tr>
<td>#pads/chip</td>
<td>1867</td>
<td>2553</td>
<td>3492</td>
<td>4776</td>
<td>6532</td>
<td>8935</td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>1250</td>
<td>2100</td>
<td>3500</td>
<td>6000</td>
<td>10000</td>
<td>16900</td>
</tr>
<tr>
<td>Chip size (mm²)</td>
<td>340</td>
<td>430</td>
<td>520</td>
<td>620</td>
<td>750</td>
<td>900</td>
</tr>
<tr>
<td>Wiring levels</td>
<td>6-7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>Power supply (V)</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>0.9</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>High-perf pow (W)</td>
<td>90</td>
<td>130</td>
<td>160</td>
<td>170</td>
<td>175</td>
<td>183</td>
</tr>
</tbody>
</table>
History #2

Von Neumann Architecture

- Read/Write Memory
  - Address
  - Data
- PE (Processing Element)

Harvard Architecture

- Program Memory
  - Address
  - Data
- Data Memory
  - Address
  - Data
- PE (Processing Element)

History #3

- Processor/memory discrepancy
  - Memory hierarchy
  - On-chip/off-chip memory
- Microprocessor execution
  - Fetch > Decode > Execute
- System on a chip - Microcontroller
  - Cost, smaller PCB, reliability, power.
  - Applications
- Evolution
  - Microprocessor
  - Microprocessor-on-a-chip
  - System-on-a-chip
  - Distributed-system-on-a-chip
History #4

- Challenges
  - scalability
    - billions of small devices
    - performance
  - availability
    - hardware changes
    - system upgrade
    - failures
    - code enhancements
  - fault tolerance

History #5

<table>
<thead>
<tr>
<th>Year</th>
<th>Processor</th>
<th>MIPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1969</td>
<td>4004</td>
<td>0.06</td>
</tr>
<tr>
<td>1970’s</td>
<td>808x</td>
<td>0.64</td>
</tr>
<tr>
<td>1982</td>
<td>286</td>
<td>1</td>
</tr>
<tr>
<td>1985</td>
<td>386</td>
<td>5</td>
</tr>
<tr>
<td>1989</td>
<td>486</td>
<td>20</td>
</tr>
<tr>
<td>1993</td>
<td>Pentium</td>
<td>100</td>
</tr>
<tr>
<td>1996</td>
<td>P II</td>
<td>250</td>
</tr>
<tr>
<td>1999</td>
<td>P III</td>
<td>500</td>
</tr>
<tr>
<td>2000</td>
<td>P 4</td>
<td>1500</td>
</tr>
</tbody>
</table>
The natural building block for multiprocessors is now also about the fastest!

Clock Frequency Growth Rate

- 30% per year
Transistor Count Growth Rate

- 100 million transistors on chip by early 2000’s A.D.
- Transistor count grows much faster than clock rate
  - 40% per year, order of magnitude more contribution in 2 decades

General Technology Trends

- Microprocessor performance increases 50%-100% per year
- Transistor count doubles every 3 years
- DRAM size quadruples every 3 years
- Huge investment per generation is carried by huge commodity market
Conventional Computer Architecture

Storage

- Divergence between memory capacity and speed more pronounced
  - Capacity increased by 1000x from 1980-95, speed only 2x
  - Gigabit DRAM by c. 2000, but gap with processor speed much greater

- Larger memories are slower, while processors get faster
  - Need to transfer more data in parallel
  - Need deeper cache hierarchies
  - How to organize caches?

<table>
<thead>
<tr>
<th>Speed</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>ns</td>
<td>~KB</td>
</tr>
<tr>
<td>10ns</td>
<td>~MB</td>
</tr>
<tr>
<td>100ns</td>
<td>~100MB</td>
</tr>
<tr>
<td>10ms</td>
<td>~10GB</td>
</tr>
<tr>
<td>&gt;100ms</td>
<td>~TB</td>
</tr>
</tbody>
</table>
Instruction Sets

- Software costs growing faster than hardware costs (1970s)
  - Machine language v.s. HLL
  - Support for high-level languages
  - Gap between high level languages and computer hardware - semantic gap
- CISC - **Complex Instruction Set Architecture**
  - Variety of instructions and addressing modes
  - DEC VAX
- HLLCA - **High Level Language Computer Architecture**

RISC Architectures

- Resolve problems using simpler architecture
  - "The case for the reduced instruction set computers" Patterson & Ditzel [1980]
- Stanford MIPS (Hennessy, 1981)
- Commercial processors: MIPS R2000 (1986), IBM RS6000, SPARC, PowerPC, etc.
- Good design methodology
- Efficient pipelining and compiler-assisted scheduling of pipeline
- Make the Common Case Fast
  - favor the frequent case
RISC Methodology

Program execution time:

\[ T = \sum n_i \cdot CPI_i \cdot T_{cycle} \]

For all instructions in the instruction set

- processor cycle time [s]
- cycles per instruction
- instruction count

80x86 Instruction Mix for SPECint92 Programs [PatHen96]

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>load</td>
<td>22</td>
</tr>
<tr>
<td>cond. branch</td>
<td>20</td>
</tr>
<tr>
<td>compare</td>
<td>16</td>
</tr>
<tr>
<td>store</td>
<td>12</td>
</tr>
<tr>
<td>add</td>
<td>8</td>
</tr>
<tr>
<td>and</td>
<td>6</td>
</tr>
<tr>
<td>sub</td>
<td>5</td>
</tr>
<tr>
<td>mov reg-reg</td>
<td>4</td>
</tr>
<tr>
<td>or</td>
<td>1</td>
</tr>
<tr>
<td>xor, not, etc.</td>
<td>1</td>
</tr>
<tr>
<td>uncond. branch</td>
<td>1</td>
</tr>
<tr>
<td>call</td>
<td>1</td>
</tr>
<tr>
<td>return, jmp indirect</td>
<td>1</td>
</tr>
<tr>
<td>shift</td>
<td>1</td>
</tr>
</tbody>
</table>
### Instruction Execution

A = B + C
result = op1 \(\text{OPERATION}\) op2

\[ A += C \]

ADD R1, M(1000)

<table>
<thead>
<tr>
<th>Mem</th>
<th>IF</th>
<th>ID</th>
<th>OF</th>
<th>EX</th>
<th>ST</th>
<th>IF</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td>1000</td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

When \(f = 5\text{MHz}\) (’70s)
- \(T_{\text{cycle}} = 200\text{ns}\)
- \(T_{\text{mem}} = 200\text{ns}\)

When \(f = 1000\text{MHz}\) (’90s)
- \(T_{\text{cycle}} = 1\text{ns}\)
- \(T_{\text{mem}} = 50\text{ns}\)

\[ \begin{align*}
3 \times 100\text{ns} &= 300\text{ns} \\
2 \times 1\text{ns} &= 2\text{ns}
\end{align*} \]

\[ 302\text{ns} \]

### Pipeline

<table>
<thead>
<tr>
<th>INSTR</th>
<th>#1</th>
<th>#2</th>
<th>#2</th>
<th>#4</th>
<th>#5</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF</td>
<td>ID</td>
<td>OF</td>
<td>EX</td>
<td>ST</td>
<td>IF</td>
</tr>
<tr>
<td>IF</td>
<td>ID</td>
<td>OF</td>
<td>EX</td>
<td>ST</td>
<td>IF</td>
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<tr>
<td>IF</td>
<td>ID</td>
<td>OF</td>
<td>EX</td>
<td>IF</td>
<td>ID</td>
</tr>
<tr>
<td>IF</td>
<td>ID</td>
<td>OF</td>
<td>IF</td>
<td>IF</td>
<td>ID</td>
</tr>
</tbody>
</table>

\[ \text{if( ) ...} \]

\[ \text{CPI} = 1 \]
System Memory

Example: 2 banks, 32 KW each, 4-byte words