

## CPE/EE 427, CPE 527 VLSI Design I: Homework 2

### 1. (30 points) Static CMOS gates

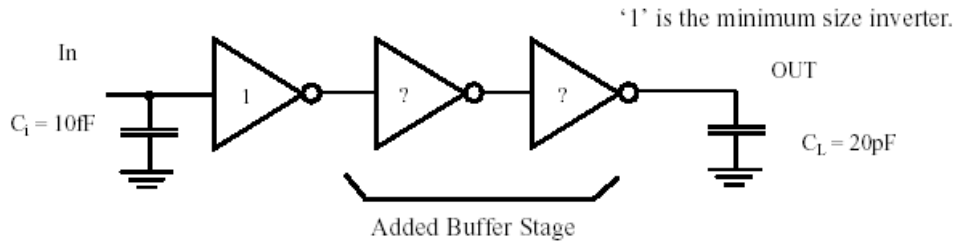
Draw transistor level schematics for the following static complementary CMOS logic cells. Clearly label the inputs (a, b, c, ...), the output (F), Vdd and Gnd. Adjust the sizes of the transistors so that n-channel and p-channel stacks have equal strengths (the same drive strength as a minimum-size CMOS inverter). Assume that logic ratio  $r=3$  ( $R_{pmin}/R_{nmin}$ ). Your implementations should occupy minimal area.

(a) (15) A gate that implements the function  $\bar{a} \cdot b + a \cdot \bar{b}$ . Complements of input signals are not available.

(b) (15) A gate that implements the function  $\overline{(a+b) \cdot c + d \cdot e \cdot f}$ .

**2. (25 points) Sizing a chain of inverters.**

**a. (10)** In order to drive a large capacitance ( $C_L = 20 \text{ pF}$ ) from a minimum size gate (with input capacitance  $C_i = 10 \text{ fF}$ ), you decide to introduce a two-staged buffer as shown in figure below. Assume that the propagation delay of a minimum size inverter is  $70 \text{ ps}$ . Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

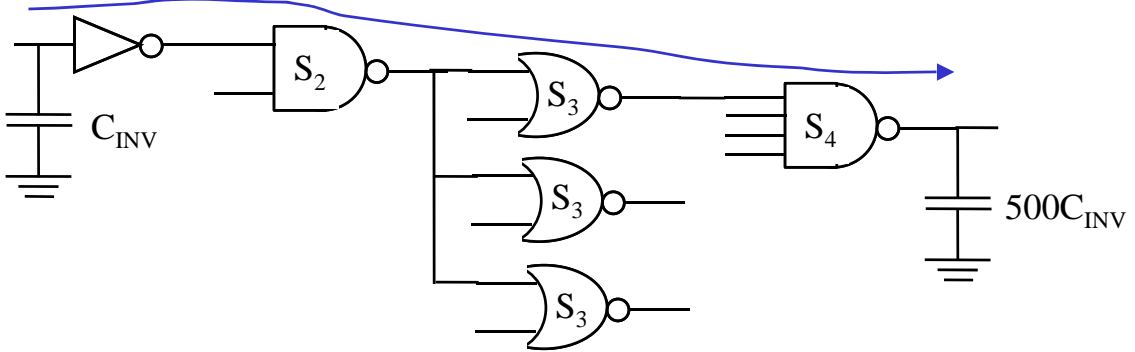


**b. (10)** If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

**c. (5)** Describe the advantages and disadvantages of the methods shown in (a) and (b).

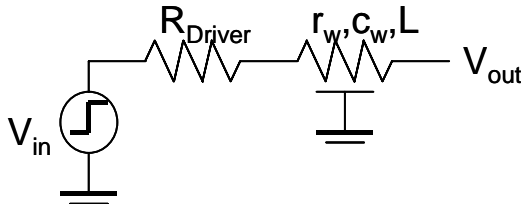
**3. (30 points) Logical Effort.**

Calculate the path optimum delay and the gate sizes.  $C_{INV}$  is the input capacitance of a minimum size inverter. Assume  $r=2$ .



#### 4. (15 points) Wires

Consider a straight Metal 2 wire in 180 nm process with the following parameters: the wire length is  $L_W = 5$  mm, the wire width is  $W_W = 0.32$   $\mu\text{m}$ , sheet resistance for Metal 2 is  $R_{\square} = 0.05\Omega/\square$ , and wire capacitance per one micrometer is  $c_W = 0.2$  fF/ $\mu\text{m}$ .



(a) (5) Calculate total wire resistance  $R_W$  and total wire capacitance  $C_W$ ?

(b) (5) Calculate total propagation delay (0-> 50%) using lumped RC model. Assume that  $R_{Driver} = 4$  K $\Omega$ .

(c) (5) Calculate total propagation delay using (0->50%) using the distributed RC model.