Fundamental Design Metrics

- Functionality
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay)
  - Power consumption; energy
- Time-to-market
Cost of Integrated Circuits

- NRE (non-recurring engineering) costs
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products
- Recurring costs – proportional to product volume
  - silicon processing
    - also proportional to chip area
  - assembly (packaging)
  - test

\[
\text{Cost per IC} = \text{Variable cost per IC} + \frac{\text{Fixed cost}}{\text{Volume}}
\]
Cost per Transistor

Fabrication capital cost per transistor (Moore's law)

Silicon Wafer

Single die

Wafer

From http://www.amd.com

Going up to 12” (30cm)
Recurring Costs

Variable cost = \( \frac{\text{Die cost} + \text{Testing cost} + \text{Packaging cost}}{\text{Final test yield}} \)

Cost of die = \( \frac{\text{Cost of wafer}}{\text{Dies per wafer} \times \text{Die yield}} \)

Dies per Wafer

\[
\text{Dies per wafer} = \pi \times \left(\frac{\text{Wafer diameter}}{2}\right)^2 - \pi \times \frac{\text{Wafer diameter}}{\sqrt{2} \times \text{Die area}}
\]
### Yield

\[
\text{Die yield} = \text{Wafer yield} \times \left(1 + \frac{\text{Defects per unit area} \times \text{Die area}}{\alpha}\right)^{-\alpha}
\]

- \(\alpha\) is approximately 3
- \(\text{die cost} = f(\text{die area})^4\)

### Examples of Cost Metrics (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Defects/cm²</th>
<th>Area (mm²)</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
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<td>115</td>
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<td>1.0</td>
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<td>66</td>
<td>27%</td>
<td>$73</td>
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<td>53</td>
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<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
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<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
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</table>
Yield Example

• Example #1:
  – 20-cm wafer for a die that is 1.5 cm on a side.
  – Solution: Die area = 1.5x1.5 = 2.25 cm².
  – Dies per wafer = 3.14x(20/2)²/2.25 – 3.14x20/(2x2.5)⁰.⁵ = 110.

• Example #2
  – Wafer size of 12 inches, die size of 2.5 cm², 1 defects/cm²,
    \( \alpha = 3 \) (measure of manufacturing process complexity)
  – 252 dies/wafer (remember, wafers round & dies square)
  – Die yield of 16%
  – 252 x 16% = only 40 dies/wafer die yield!

• Die cost is strong function of die area
  – proportional to the third or fourth power of the die area

Functionality and Robustness

• Prime requirement –
  IC performs the function it is designed for

• Normal behavior deviates due to
  – variations in the manufacturing process (dimensions and device parameters vary between runs and even on a single wafer or die)
  – presence of disturbing on- or off-chip noise sources

• Noise: Unwanted variation of voltages or currents at the logic nodes
Reliability
Noise in Digital Integrated Circuits

- Inductive coupling
  - current change on one wire can influence signal on the neighboring wire
- Capacitive coupling
  - voltage change on one wire can influence signal on the neighboring wire
  - cross talk

• from two wires placed side by side
  - inductive coupling
• from noise on the power and ground supply rails
  - can influence signal levels in the gate

Example of Capacitive Coupling

• Signal wire glitches as large as 80% of the supply voltage will be common due to crosstalk between neighboring wires as feature sizes continue to scale

Crosstalk vs. Technology

- Black line quiet
- Red lines pulsed
- Glitches strength vs technology

From Dunlop, Lucent, 2000
Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables $x \in \{0,1\}$
- A logical variable is associated with a *nominal voltage level* for each logic state
  
  \[
  1 \leftrightarrow V_{OH} \quad \text{and} \quad 0 \leftrightarrow V_{OL}
  \]
- Difference between $V_{OH}$ and $V_{OL}$ is the logic or *signal swing* $V_{sw}$

DC Operation

**Voltage Transfer Characteristic**

\[
V_{OH} = f(V_{OL}) \\
V_{OL} = f(V_{OH}) \\
V_{M} = f(V_{M})
\]

Switching Threshold
Mapping between analog and digital signals

- The regions of acceptable high and low voltages are delimited by \( V_{IH} \) and \( V_{IL} \) that represent the points on the VTC curve where the gain = -1 (\( dV_{out}/dV_{in} \)).

```
+--------------+-----------------+
|             | VOH             |
|             | VIL             |
|             | Undefined Region|
+--------------+-----------------+
```

```
+--------------+-----------------+
|             | VOH             |
|             | VIL             |
|             | VOL             |
+--------------+-----------------+
```

```
Vout
```

Definition of Noise Margins

- For robust circuits, want the “0” and “1” intervals to be as large as possible.

```
VDD
```

```
VDD
```

```
Gnd
```

```
Gate Output
```

```
Gate Input
```

```
NM_H = V_{OH} - V_{IH}
```

```
NM_L = V_{IL} - V_{OL}
```

- Large noise margins are desirable, but not sufficient …
The Regenerative Property

- A gate with regenerative property ensures that a disturbed signal converges back to a nominal voltage level.

![Diagram showing the regenerative property](image)

Conditions for Regeneration

- To be regenerative, the VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.

![Diagram showing conditions for regeneration](image)
**Noise Immunity**

- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, crosstalk, interference, offset
- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between $V_{OH}$ and $V_{OL}$) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

**Directivity**

- A gate must be *undirectional*: changes in an output level should not appear at any unchanging input of the same circuit
  - In real circuits *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)
- Key metrics: *output impedance* of the driver and *input impedance* of the receiver
  - ideally, the output impedance of the driver should be zero
  - input impedance of the receiver should be infinity
**Fan-In and Fan-Out**

- **Fan-out** – number of load gates connected to the output of the driving gate
  - gates with large fan-out are slower

- **Fan-in** – the number of inputs to the gate
  - gates with large fan-in are bigger and slower

**The Ideal Inverter**

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.

\[ g = -\infty \]

\[ R_i = \infty \]

\[ R_o = 0 \]

\[ \text{Fanout} = \infty \]

\[ \text{NM}_{H} = \text{NM}_{L} = \text{VDD}/2 \]
An Old-time Inverter

Delay Definitions
Delay Definitions

- \( V_{in} \rightarrow V_{out} \)
- \( V_{out} \)
- \( V_{in} \)
- Input waveform
- Output waveform
- Propagation delay
- \( t_p = (t_{pHL} + t_{pLH})/2 \)

Modeling Propagation Delay

- Model circuit as first-order RC network

\[
v_{out}(t) = (1 - e^{-t/\tau})V
\]

where \( \tau = RC \)

- Time to reach 50% point is
  \[
  t = \ln(2) \tau = 0.69 \tau
  \]

- Time to reach 90% point is
  \[
  t = \ln(9) \tau = 2.2 \tau
  \]

- Matches the delay of an inverter gate
Power and Energy Dissipation

- Power consumption: how much energy is consumed per operation and how much heat the circuit dissipates
  - supply line sizing (determined by peak power)
    \[ P_{\text{peak}} = V_{dd} I_{\text{peak}} \]
  - battery lifetime (determined by average power dissipation)
    \[ P_{\text{avg}} = 1/T \int p(t) \, dt = \frac{V_{dd}}{T} \int i_{dd}(t) \, dt \]
  - packaging and cooling requirements

- Two important components: static and dynamic

\[
E \text{ (joules)} = C_L V_{dd}^2 P_{0\rightarrow1} + t_{sc} V_{dd} I_{\text{peak}} P_{0\rightarrow1} + V_{dd} I_{\text{leakage}}
\]

\[
P \text{ (watts)} = C_L V_{dd}^2 f_{0\rightarrow1} + t_{sc} V_{dd} I_{\text{peak}} f_{0\rightarrow1} + V_{dd} I_{\text{leakage}}
\]

Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate

- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
  - Power-delay product (PDP) – energy consumed by the gate per switching event

- An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is
  - Energy-delay product (EDP) = power-delay \(^2\)
Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this course
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation

The MOS Transistor

![Diagram of MOS Transistor]

- Polysilicon
- Aluminum
- Gate Oxide
- Field Oxide
- Source/Drain Regions
- P-Type
- N+
The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration $N_D$ - electrons are the majority carriers

p areas have been doped with acceptor ions (boron) of concentration $N_A$ - holes are the majority carriers

Switch Model of NMOS Transistor

$|V_{GS}| < |V_T|$ (Open (off) (Gate = ‘0’))

$|V_{GS}| > |V_T|$ (Closed (on) (Gate = ‘1’))
Switch Model of PMOS Transistor

\[ |V_{GS}| > |V_{DD} - |V_T|| \]  
Open (off) (Gate = ‘1’)

\[ |V_{GS}| < |V_{DD} - |V_T|| \]  
Closed (on) (Gate = ‘0’)

CMOS Inverter: A First Look

\[ V_{DD} \]
\[ V_{in} \]
\[ V_{out} \]
\[ C_L \]
CMOS Inverter: Steady State Response

\[ V_{DD} \]
\[ R_p \]
\[ V_{out} = 1 \]
\[ V_{in} = 0 \]

\[ V_{DD} \]
\[ R_n \]
\[ V_{out} = 0 \]
\[ V_{in} = V_{DD} \]

\[ V_{OH} = V_{DD} \]
\[ V_{OL} = 0 \]
\[ V_M = f(R_p, R_n) \]

Growing the Silicon Ingot

From Smithsonian, 2000

8/31/2005  VLSI Design I; A. Milenkovic 37

8/31/2005  VLSI Design I; A. Milenkovic 38
CMOS Process at a Glance

- Define active areas
- Etch and fill trenches
- Implant well regions
- Deposit and pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact and via windows
- Deposit and pattern metal layers

- One full photolithography sequence per layer (mask)
- Built (roughly) from the bottom up
  - 5 metal 2
  - 4 metal 1
  - 2 polysilicon
  - 3 source and drain diffusions
  - 1 tubs (aka wells, active areas)

Photolithographic Process

- Oxidation
- Optical mask
- Process step
- Photoresist removal (ashing)
- Photoresist coating
- Exposure
- Acid etch
- Spin, rinse, dry
Patterning - Photolithography

1. Oxidation
2. Photoresist (PR) coating
3. Stepper exposure
4. Photoresist development and bake
5. Acid etching
   - Unexposed (negative PR)
   - Exposed (positive PR)
6. Spin, rinse, and dry
7. Processing step
   - Ion implantation
   - Plasma etching
   - Metal deposition
8. Photoresist removal (ashing)

Example of Patterning of SiO2

1. After oxidation and deposition of negative photoresist
2. UV-light
3. Stepper exposure
4. After development and etching of resist, chemical or plasma etch of SiO2
5. After etching
6. Chemical or plasma etch
7. Si-substrate
8. Final result after removal of resist
Diffusion and Ion Implantation

1. Area to be doped is exposed (photolithography)

2. Diffusion or Ion implantation

Deposition and Etching

1. Pattern masking (photolithography)

2. Deposit material over entire wafer
   - CVD (Si₃N₄)
   - chemical deposition (polysilicon)
   - sputtering (Al)

3. Etch away unwanted material
   - wet etching
   - dry (plasma) etching
Planarization: Polishing the Wafers

Self-Aligned Gates

1. Create thin oxide in the “active” regions, thick elsewhere

2. Deposit polysilicon

3. Etch thin oxide from active region (poly acts as a mask for the diffusion)

4. Implant dopant
Simplified CMOS Inverter Process

cut line

P-Well Mask
Contact Mask

Metal Mask
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS

Modern CMOS Process Walk-Through

Base material: p+ substrate with p-epi layer

After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

After plasma etch of insulating trenches using the inverse of the active area mask
CMOS Process Walk-Through, con’t

**After trench filling, CMP planarization, and removal of sacrificial nitride**

After n-well and $V_{TP}$ adjust implants

After p-well and $V_{TN}$ adjust implants

**CMOS Process Walk-Through, con’t**

After polysilicon deposition and etch

After $n^+$ source/drain and $p^+$ source/drain implants. These steps also dope the polysilicon.

After deposition of SiO$_2$ insulator and contact hole etch
CMOS Process Walk-Through, con’t

After deposition and patterning of first Al layer.

After deposition of SiO₂ insulator, etching of via’s, deposition and patterning of second layer of Al.

Layout Editor: max Design Frame
**max Layer Representation**

- Metals (five) and vias/contacts between the interconnect levels
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support "stacked vias"
- Active – active areas on/in substrate (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))
- Wells (nw) and other select areas (pplus, nplus, prb)

---

**CMOS Inverter max Layout**

- NMOS (2/.24 = 8/1)
- PMOS (4/.24 = 16/1)
- metal1-poly via
- metal1-diff via
- metal2-metal1 via
- GND
- VDD
- In
- Out
Simplified Layouts in \textit{max}

- Online design rule checking (DRC)
- Automatic fet generation (just overlap poly and diffusion and it creates a transistor)
- Simplified via/contact generation
  - v12, v23, v34, v45
  - ct, nwc, pwc

\begin{center}
\includegraphics[width=0.5\textwidth]{simplified_layouts.png}
\end{center}

Design Rule Checker

\begin{center}
\includegraphics[width=0.5\textwidth]{design_rule_checker.png}
\end{center}
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

To be able to tolerate some level of fabrication errors such as

1. Mask misalignment
2. Dust
3. Process parameters (e.g., lateral diffusion)
4. Rough surfaces
Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are not related) on the same layer to ensure they will not short after fab

Intra-Layer Design Rules
Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers

- Transistors
  - Catastrophic error

- Unrelated Poly & Diffusion
  - Thinner diffusion, but still working

Transistor Layout

- Transistor
  - 1
  - 2
  - 3
  - 4
  - 5
Select Layer

Inter-Layer Design Rule Origins, Con’t

2. Contact and via rules

M1 contact to p-diffusion
M1 contact to n-diffusion
M1 contact to poly
Mx contact to My

Contact Mask

Via Masks

both materials

Contact: 0.44 x 0.44

mask misaligned
Vias and Contacts

CMOS Process Layers

<table>
<thead>
<tr>
<th>Mask/Layer name</th>
<th>Derivation from drawn layers</th>
<th>Alternative names for mask/layer</th>
<th>MOSIS mask label</th>
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<tr>
<td>n-well</td>
<td>n-well</td>
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<td>COG</td>
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To probe further

• http://www.leb.e-technik.uni-erlangen.de/lehre/mm/html/start.htm