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**CPE/EE 427, CPE 527  
VLSI Design I  
L04: MOS Transistors Theory**

Department of Electrical and Computer Engineering  
University of Alabama in Huntsville

Aleksandar Milenkovic ( [www.ece.uah.edu/~milenka](http://www.ece.uah.edu/~milenka) )  
[www.ece.uah.edu/~milenka/cpe527-05F](http://www.ece.uah.edu/~milenka/cpe527-05F)

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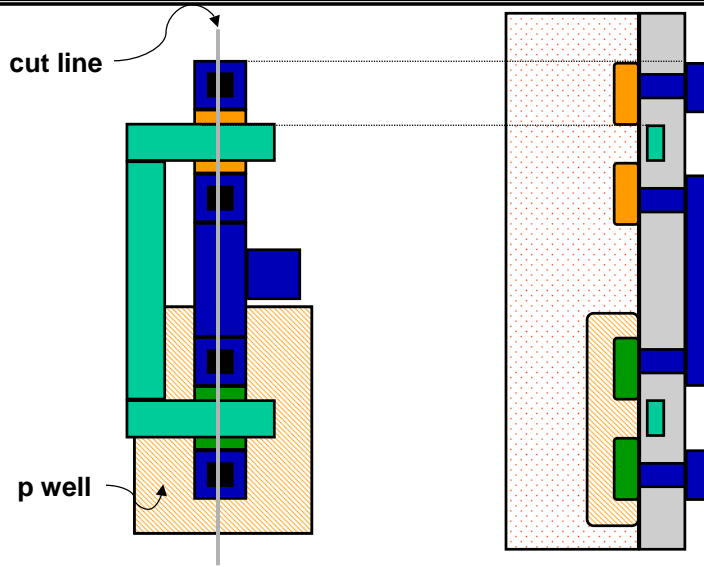
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### Course Administration

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- Instructor: Aleksandar Milenkovic  
[milenka@ece.uah.edu](mailto:milenka@ece.uah.edu)  
[www.ece.uah.edu/~milenka](http://www.ece.uah.edu/~milenka)  
EB 217-L  
Mon. 5:30 PM – 6:30 PM,  
Wen. 12:30 – 13:30 PM
- URL: <http://www.ece.uah.edu/~milenka/cpe527-05F>
- TA: Joel Wilder
- Labs: Lab#1 this week
- Text: CMOS VLSI Design, 3<sup>rd</sup> ed., Weste, Harris
- Review: Introduction, Design Metrics, IC Fabrication  
(Read Chapter 1); IC Fabrication (Chapter 3)
- Today: MOS Transistor Theory (Chapter 2)

## Review: Simplified CMOS Inverter Process

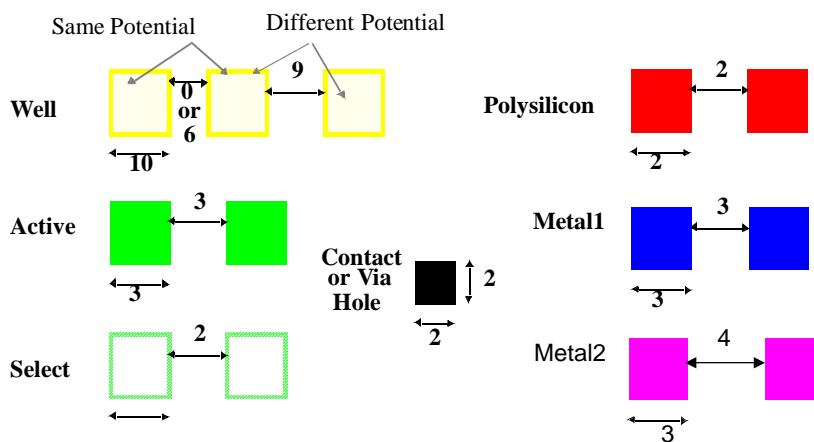


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## Review: Intra-Layer Design Rules



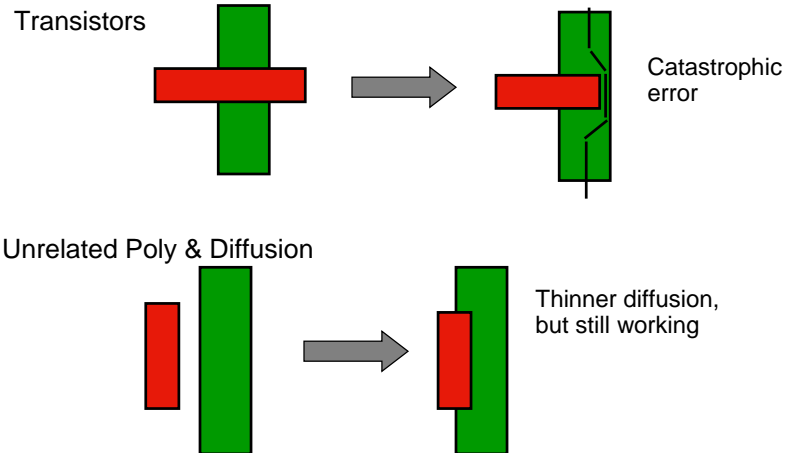
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## Review: Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers

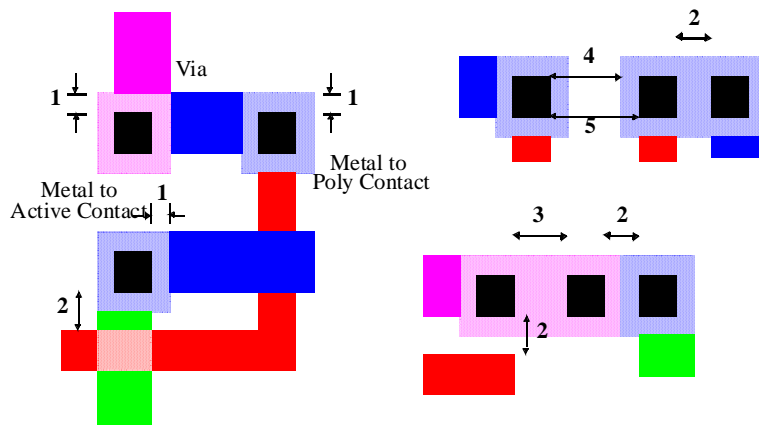


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## Review: Vias and Contacts



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## Outline

- Introduction
- MOS Capacitor
- nMOS I-V Characteristics
- pMOS I-V Characteristics
- Gate and Diffusion Capacitance
- Non-Ideal IV Effects

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## Introduction

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C / I) \Delta V$
  - Capacitance and current determine speed
- Also explore what a “degraded level” really means



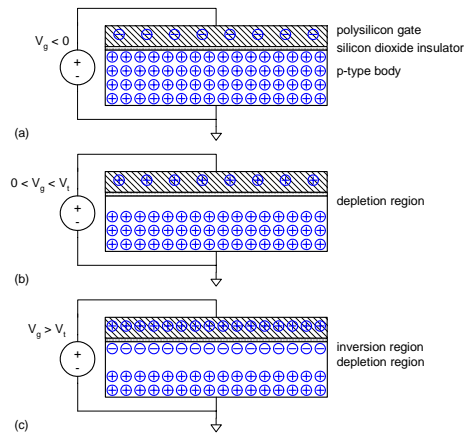
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## MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



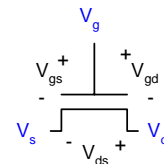
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## Terminal Voltages

- Mode of operation depends on  $V_g$ ,  $V_d$ ,  $V_s$ 
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence  $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



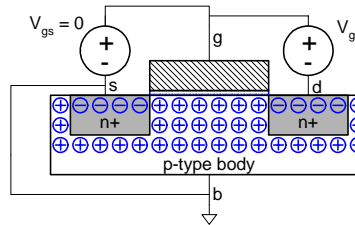
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## nMOS Cutoff

- No channel
- $I_{ds} = 0$



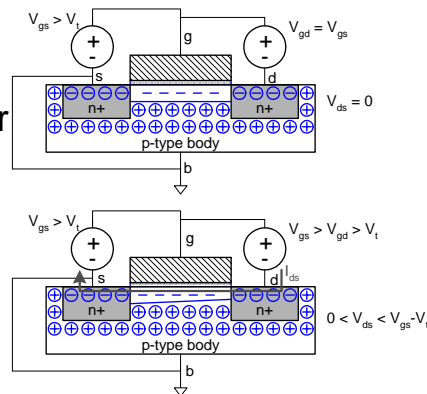
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## nMOS Linear

- Channel forms
- Current flows from d to s
  - $e^-$  from s to d
- $I_{ds}$  increases with  $V_{ds}$
- Similar to linear resistor



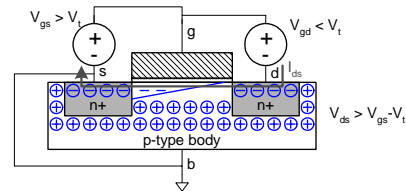
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## nMOS Saturation

- Channel pinches off
- $I_{ds}$  independent of  $V_{ds}$
- We say current saturates
- Similar to current source



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## I-V Characteristics

- In Linear region,  $I_{ds}$  depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

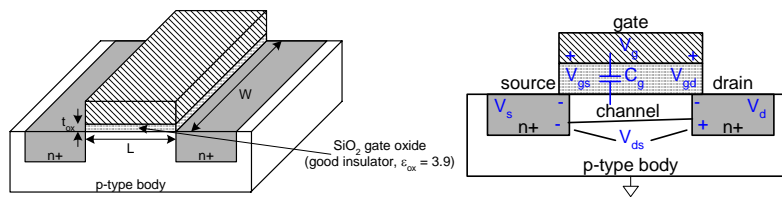
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## Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} =$



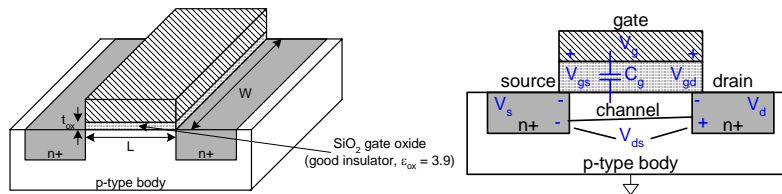
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## Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C =$



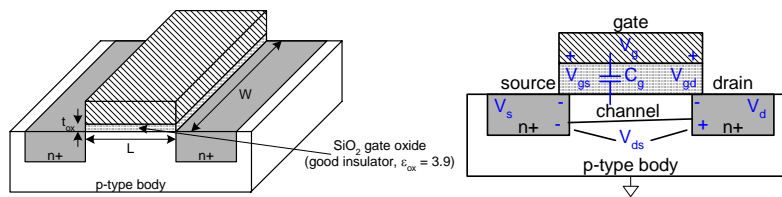
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## Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C = C_g = \epsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}} WL$   $C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$
- $V =$



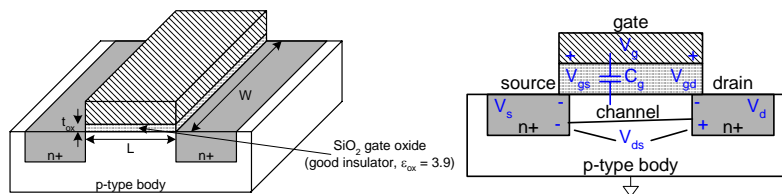
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## Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C = C_g = \epsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}} WL$   $C_{\text{ox}} = \epsilon_{\text{ox}} / t_{\text{ox}}$
- $V = V_{\text{gc}} - V_t = (V_{\text{gs}} - V_{\text{ds}}/2) - V_t$



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## Carrier velocity

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- Charge is carried by e-
- Carrier velocity  $v$  proportional to lateral E-field between source and drain
- $v =$

## Carrier velocity

---

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- Carrier velocity  $v$  proportional to lateral E-field between source and drain
- $v = \mu E$        $\mu$  called mobility
- $E =$

## Carrier velocity

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- Charge is carried by e-
- Carrier velocity  $v$  proportional to lateral E-field between source and drain
- $v = \mu E$        $\mu$  called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t =$

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## Carrier velocity

---

- Charge is carried by e-
- Carrier velocity  $v$  proportional to lateral E-field between source and drain
- $v = \mu E$        $\mu$  called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

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## nMOS Linear I-V

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- Now we know
  - How much charge  $Q_{\text{channel}}$  is in the channel
  - How much time  $t$  each carrier takes to cross

$$I_{ds} =$$

## nMOS Linear I-V

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- Now we know
  - How much charge  $Q_{\text{channel}}$  is in the channel
  - How much time  $t$  each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$
$$=$$

## nMOS Linear I-V

- Now we know
  - How much charge  $Q_{\text{channel}}$  is in the channel
  - How much time  $t$  each carrier takes to cross

$$\begin{aligned} I_{ds} &= \frac{Q_{\text{channel}}}{t} \\ &= \mu C_{\text{ox}} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \\ &= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \end{aligned} \quad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

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## nMOS Saturation I-V

- If  $V_{gd} < V_t$ , channel pinches off near drain
  - When  $V_{ds} > V_{\text{dsat}} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} =$$

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## nMOS Saturation I-V

- If  $V_{gd} < V_t$ , channel pinches off near drain
  - When  $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$$

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## nMOS Saturation I-V

- If  $V_{gd} < V_t$ , channel pinches off near drain
  - When  $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$\begin{aligned} I_{ds} &= \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat} \\ &= \frac{\beta}{2} (V_{gs} - V_t)^2 \end{aligned}$$

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## nMOS I-V Summary

- Shockley 1<sup>st</sup> order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

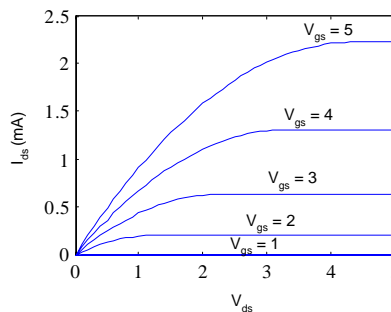
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## Example

- For a 0.6  $\mu\text{m}$  process
  - From AMI Semiconductor
  - $t_{\text{ox}} = 100 \text{ \AA}$
  - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
  - $V_t = 0.7 \text{ V}$
- Plot  $I_{ds}$  vs.  $V_{ds}$ 
  - $V_{gs} = 0, 1, 2, 3, 4, 5$
  - Use  $W/L = 4/2 \lambda$



$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left( \frac{3.9 \cdot 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left( \frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A}/\text{V}^2$$

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## pMOS I-V

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- All dopings and voltages are inverted for pMOS
- Mobility  $\mu_p$  is determined by holes
  - Typically 2-3x lower than that of electrons  $\mu_n$
  - 120 cm<sup>2</sup>/V\*s in AMI 0.6  $\mu$ m process
- Thus pMOS must be wider to provide same current
  - In this class, assume  $\mu_n / \mu_p = 2$
  
  - \*\*\* plot I-V here

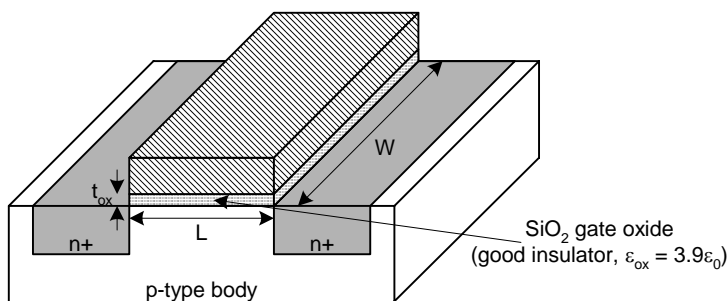
## Capacitance

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- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

## Gate Capacitance (simple model)

- Approximate channel as connected to source
- $C_{gs} = \epsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W$
- $C_{permicron}$  is typically about 2 fF/ $\mu\text{m}$



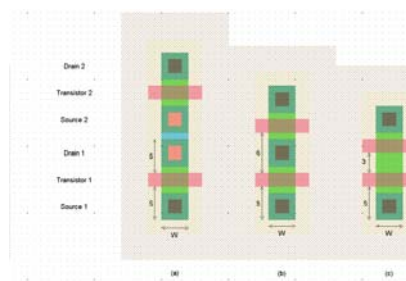
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## Diffusion Capacitance (simple model)

- $C_{sb}$ ,  $C_{db}$
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to  $C_g$  for contacted diff
  - $\frac{1}{2} C_g$  for uncontacted
  - Varies with process

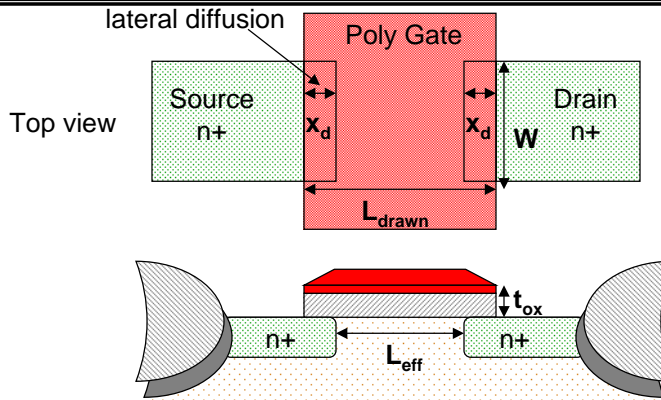


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## MOS Structure Capacitances



Overlap capacitance (linear)

$$C_{GSO} = C_{GDO} = C_{ox} x_d W = C_o W$$

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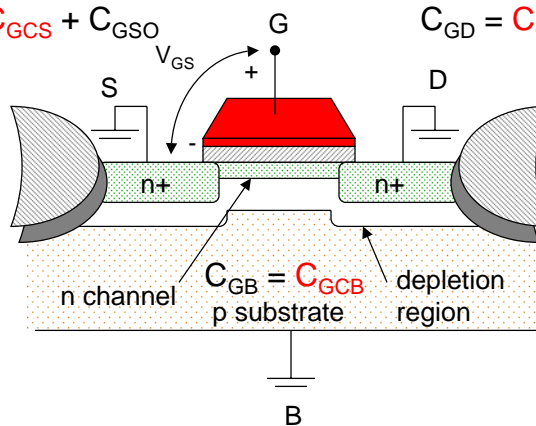
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## MOS Channel Capacitances

- The gate-to-channel capacitance depends upon the operating region and the terminal voltages

$$C_{GS} = C_{GCS} + C_{GSO} \quad C_{GD} = C_{GCD} + C_{GDO}$$



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## Average Distribution of Channel Capacitance

Operation Region	$C_{GCB}$	$C_{GCS}$	$C_{GCD}$	$C_{GC}$	$C_G$
Cutoff	$C_{ox}WL$	0	0	$C_{ox}WL$	$C_{ox}WL + 2C_0W$
Resistive	0	$C_{ox}WL/2$	$C_{ox}WL/2$	$C_{ox}WL$	$C_{ox}WL + 2C_0W$
Saturation	0	$(2/3)C_{ox}WL$	0	$(2/3)C_{ox}WL$	$(2/3)C_{ox}WL + 2C_0W$

- Channel capacitance components are nonlinear and vary with operating voltage
- Most important regions are cutoff and saturation since that is where the device spends most of its time

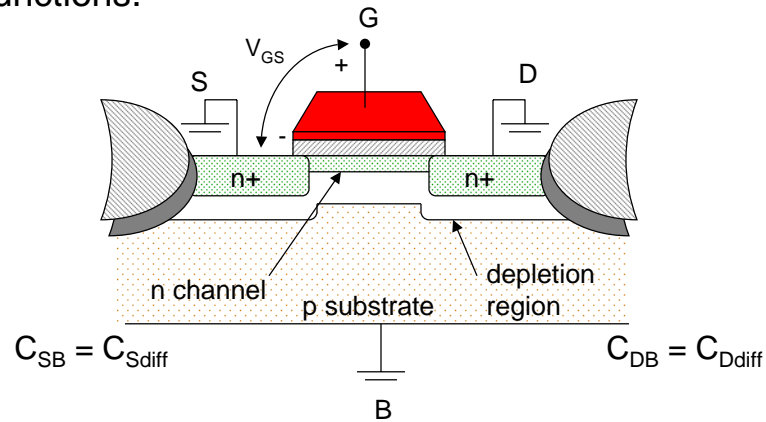
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## MOS Diffusion Capacitances

- The junction (or diffusion) capacitance is from the reverse-biased source-body and drain-body pn-junctions.

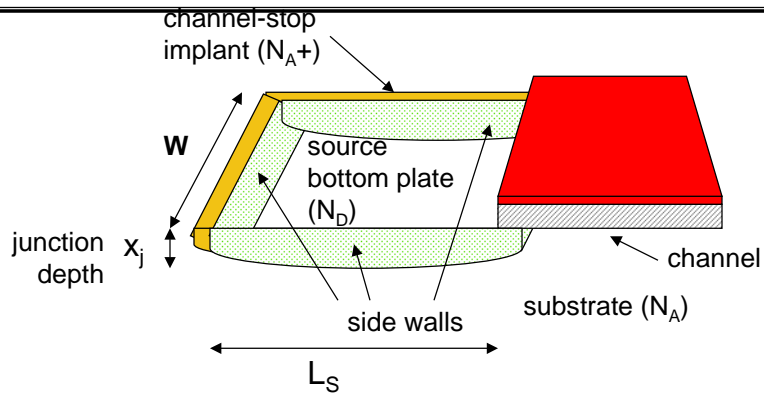


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## Source Junction View



$$C_{diff} = C_{bp} + C_{sw} = C_j \text{ AREA} + C_{jsw} \text{ PERIMETER}$$

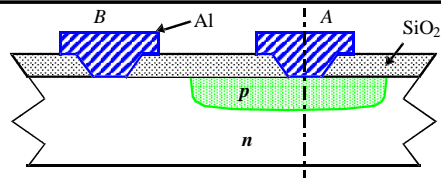
$$= C_j L_S W + C_{jsw} (2L_S + W)$$

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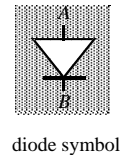
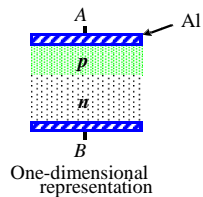
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## Recap: The Diode



Cross-section of  $pn$  junction in an IC process



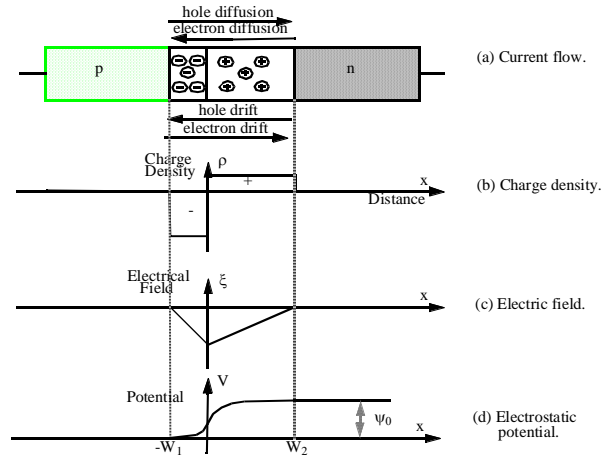
*Mostly occurring as parasitic element in Digital ICs*

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## Recap: Depletion Region

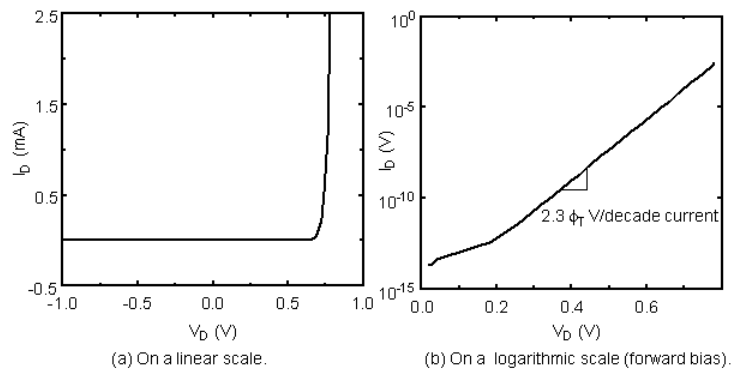


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## Recap: Diode Current



$$I_D = I_S (e^{V_D/\phi_T} - 1)$$

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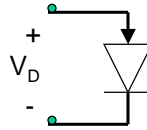
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## Recap: Ideal Diode Equation

- The *ideal diode equation* (for both forward and reverse-bias conditions) is

$$I_D = I_S(e^{V_D/\phi_T} - 1)$$

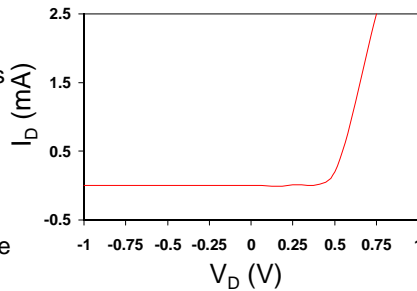


where  $V_D$  is the voltage applied to the junction

- a forward-bias lowers the potential barrier allowing carriers to flow across the diode junction
- a reverse-bias raises the potential barrier and the diode becomes nonconducting

$$\phi_T = kT/q = 26\text{mV at } 300\text{K}$$

$I_S$  is the saturation current of the diode



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## MOS Diffusion Capacitances

$$C_{\text{diff}} = C_{\text{bp}} + C_{\text{sw}} = C_{\text{jbp}} \text{ AREA} + C_{\text{jsw}} \text{ PERIMETER}$$

$$= C_{\text{jbp}} L_S W + C_{\text{jsw}} (2L_S + W)$$

Source parasitic:

$$C_{\text{jbs}} = C_J(1 + V_{\text{sb}}/\psi_0)^{-M_j}$$

$C_J$  – junction capacitance at zero bias

$M_j$  – junction grading coefficient (0.5 – 0.33)

$\psi_0$  – built-in potential  $\{\psi_0 = v_T \ln(N_A N_D / n_i^2)\}$

$$C_{\text{jbsw}} = C_{\text{JSW}}(1 + V_{\text{sb}}/\psi_0)^{-M_{\text{jsw}}}$$

$C_{\text{JSW}}$  – junction capacitance at zero bias

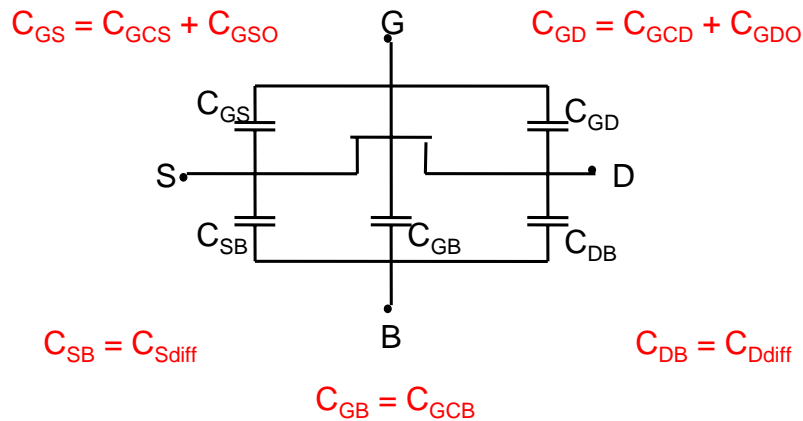
$M_{\text{jsw}}$  – junction grading coefficient (0.5 – 0.33)

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## MOS Capacitance Model



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## Transistor Capacitance Values for 0.25 $\mu$

Example: For an NMOS with  $L = 0.24 \mu\text{m}$ ,  $W = 0.36 \mu\text{m}$ ,  $L_D = L_S = 0.625 \mu\text{m}$

$$C_{GSO} = C_{GDO} = C_{ox} \times d \times W = C_o \times W =$$

$$C_{GC} = C_{ox} \times WL =$$

$$\text{so } C_{gate\_cap} = C_{ox} \times WL + 2C_o \times W =$$

$$C_{bp} = C_j \times L_S \times W =$$

$$C_{sw} = C_{jsw} \times (2L_S + W) =$$

$$\text{so } C_{diffusion\_cap} =$$

	$C_{ox}$ (fF/ $\mu\text{m}^2$ )	$C_o$ (fF/ $\mu\text{m}$ )	$C_j$ (fF/ $\mu\text{m}^2$ )	$m_j$	$\phi_b$ (V)	$C_{jsw}$ (fF/ $\mu\text{m}$ )	$m_{jsw}$	$\phi_{bsw}$ (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

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## Transistor Capacitance Values for 0.25 $\mu$

Example: For an NMOS with  $L = 0.24 \mu\text{m}$ ,  $W = 0.36 \mu\text{m}$ ,

$$L_D = L_S = 0.625 \mu\text{m}$$

$$C_{GSO} = C_{GDO} = C_{ox} x_d W = C_o W = 0.11 \text{ fF}$$

$$C_{GC} = C_{ox} WL = 0.52 \text{ fF}$$

$$\text{so } C_{\text{gate\_cap}} = C_{ox}WL + 2C_oW = 0.74 \text{ fF}$$

$$C_{bp} = C_j L_S W = 0.45 \text{ fF}$$

$$C_{sw} = C_{jsw} (2L_S + W) = 0.45 \text{ fF}$$

$$\text{so } C_{\text{diffusion\_cap}} = 0.90 \text{ fF}$$

	$C_{ox}$ (fF/ $\mu\text{m}^2$ )	$C_o$ (fF/ $\mu\text{m}$ )	$C_j$ (fF/ $\mu\text{m}^2$ )	$m_j$	$\phi_b$ (V)	$C_{jsw}$ (fF/ $\mu\text{m}$ )	$m_{jsw}$	$\phi_{bsw}$ (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

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## Non-Ideal I-V Effects

- $I_{ds}(\text{sat})$  increases less than quadratically with increasing  $V_{gs}$

- Velocity saturation & mobility degradation

- $I_{ds}(\text{sat})$  increases slightly with  $V_{ds}$

- Channel length modulation

- $V_T$  is influenced by the  $V_{sb}$

- Body effect

- There is current flow in nominally OFF transistors

- Subthreshold conduction (junction leakage, tunnel)

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

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## Current Determinates

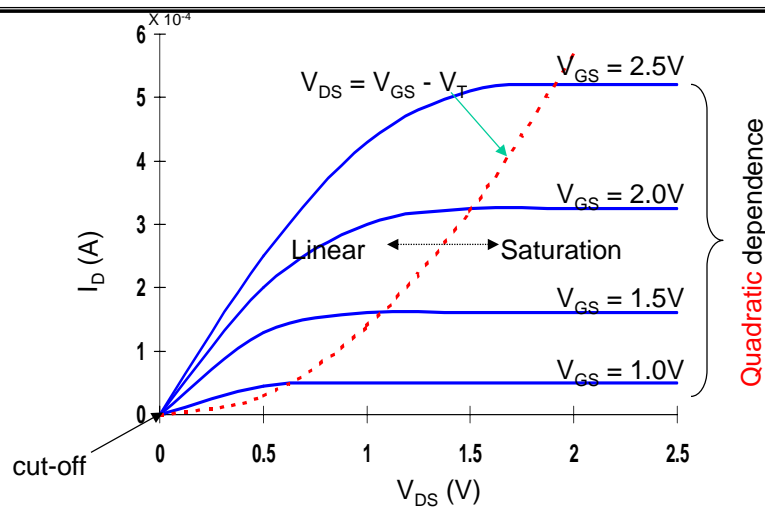
- For a fixed  $V_{DS}$  and  $V_{GS} (> V_T)$ ,  $I_{DS}$  is a function of
  - the distance between the source and drain –  $L$
  - the channel width –  $W$
  - the threshold voltage –  $V_T$
  - the thickness of the  $\text{SiO}_2$  –  $t_{ox}$
  - the dielectric of the gate insulator ( $\text{SiO}_2$ ) –  $\epsilon_{ox}$
  - the carrier mobility
    - for nfets:  $\mu_n = 500 \text{ cm}^2/\text{V-sec}$
    - for pfets:  $\mu_p = 180 \text{ cm}^2/\text{V-sec}$

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## Long Channel I-V Plot (NMOS)



NMOS transistor,  $0.25\mu\text{m}$ ,  $L_d = 10\mu\text{m}$ ,  $W/L = 1.5$ ,  $V_{DD} = 2.5\text{V}$ ,  $V_T = 0.4\text{V}$

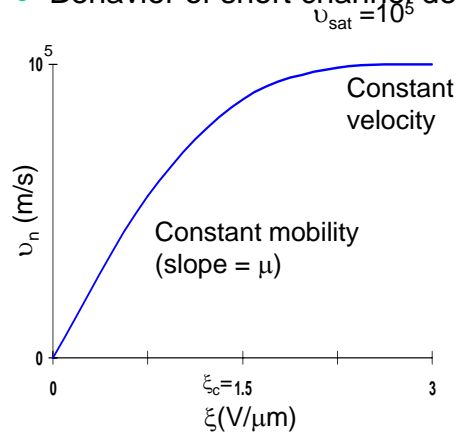
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## Short Channel Effects

- Behavior of short channel device mainly due to



- Velocity saturation** – the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

- For an NMOS device with  $L$  of  $.25\mu\text{m}$ , only a couple of volts difference between  $D$  and  $S$  are needed to reach velocity saturation

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## Voltage-Current Relation: Velocity Saturation

For short channel devices

- Linear: When  $V_{\text{DS}} \leq V_{\text{GS}} - V_{\text{T}}$

$$I_{\text{D}} = \kappa(V_{\text{DS}}) k'_{\text{n}} W/L [(V_{\text{GS}} - V_{\text{T}})V_{\text{DS}} - V_{\text{DS}}^2/2]$$

where

$\kappa(V) = 1/(1 + (V/\xi_{\text{c}}L))$  is a measure of the degree of velocity saturation

- Saturation: When  $V_{\text{DS}} = V_{\text{DSAT}} \geq V_{\text{GS}} - V_{\text{T}}$

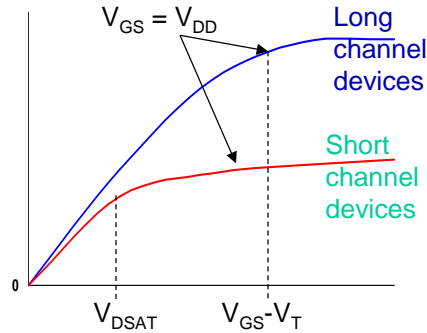
$$I_{\text{DSat}} = \kappa(V_{\text{DSAT}}) k'_{\text{n}} W/L [(V_{\text{GS}} - V_{\text{T}})V_{\text{DSAT}} - V_{\text{DSAT}}^2/2]$$

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## Velocity Saturation Effects



For short channel devices and large enough  $V_{GS} - V_T$

- $V_{DSAT} < V_{GS} - V_T$  so the device enters saturation **before**  $V_{DS}$  reaches  $V_{GS} - V_T$  and operates more often in saturation

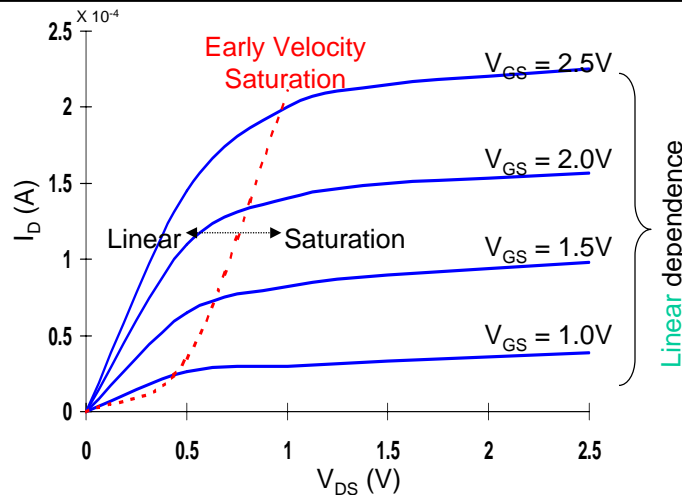
- $I_{DSAT}$  has a **linear dependence** wrt  $V_{GS}$  so a reduced amount of current is delivered for a given control voltage

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## Short Channel I-V Plot (NMOS)



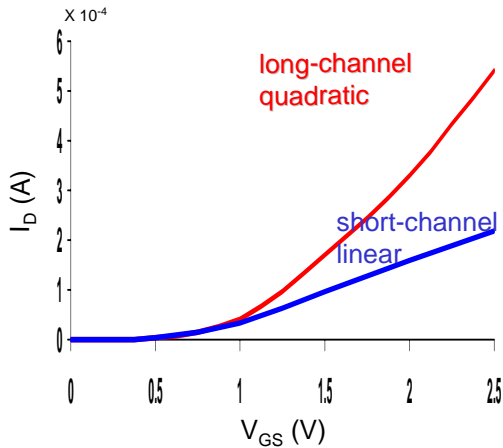
NMOS transistor,  $0.25\mu m$ ,  $L_d = 0.25\mu m$ ,  $W/L = 1.5$ ,  $V_{DD} = 2.5V$ ,  $V_T = 0.4V$

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## MOS $I_D$ - $V_{GS}$ Characteristics



- Linear (short-channel) versus quadratic (long-channel) dependence of  $I_D$  on  $V_{GS}$  in saturation

- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of  $V_{DS}$  resulting in a substantial drop in current drive

(for  $V_{DS} = 2.5V$ ,  $W/L = 1.5$ )

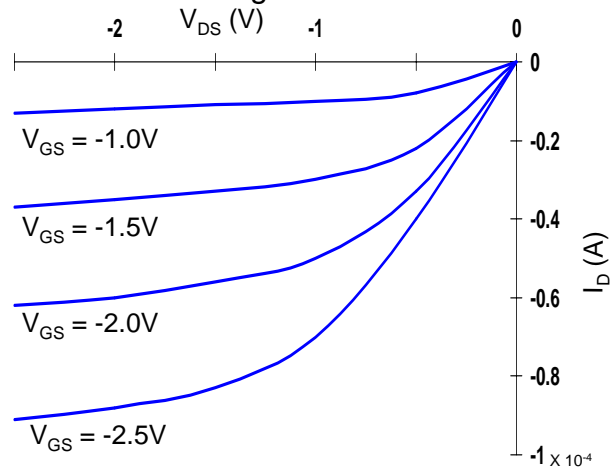
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## Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed



PMOS transistor,  $0.25\mu m$ ,  $L_d = 0.25\mu m$ ,  $W/L = 1.5$ ,  $V_{DD} = 2.5V$ ,  $V_T = -0.4V$

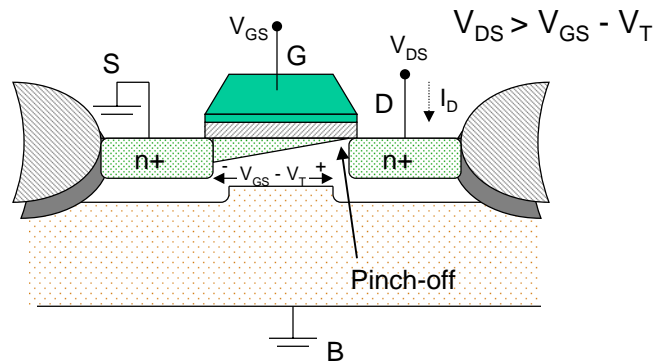
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## Transistor in Saturation Mode

Assuming  $V_{GS} > V_T$



The current remains constant (saturates).

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## Voltage-Current Relation: Saturation Mode

For long channel devices

- When  $V_{DS} \geq V_{GS} - V_T$

$$I_D' = k_n' / 2 \cdot W/L [(V_{GS} - V_T)^2]$$

since the voltage difference over the induced channel (from the **pinch-off** point to the source) remains fixed at  $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied  $V_{DS}$ , so

$$I_D = I_D' (1 + \lambda V_{DS})$$

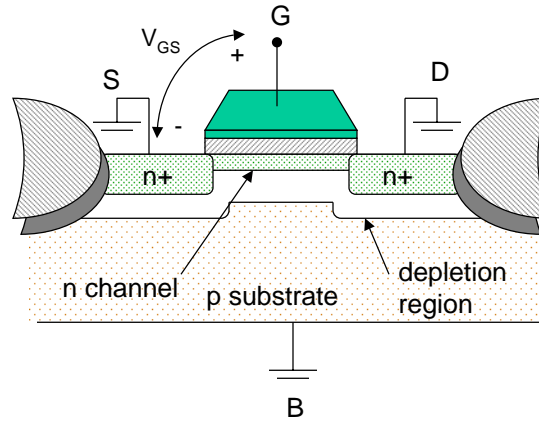
where  $\lambda$  is the **channel-length modulation** (varies with the inverse of the channel length)

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## Threshold Voltage Concept



The value of  $V_{GS}$  where strong inversion occurs is called the threshold voltage,  $V_T$

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## The Threshold Voltage

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

where

$V_{T0}$  is the threshold voltage at  $V_{SB} = 0$  and is mostly a function of the manufacturing process

- Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

$V_{SB}$  is the source-bulk voltage

$\phi_F = -\phi_T \ln(N_A/n_i)$  is the **Fermi potential** ( $\phi_T = kT/q = 26\text{mV}$  at 300K is the thermal voltage;  $N_A$  is the acceptor ion concentration;  $n_i \approx 1.5 \times 10^{10} \text{ cm}^{-3}$  at 300K is the intrinsic carrier concentration in pure silicon)

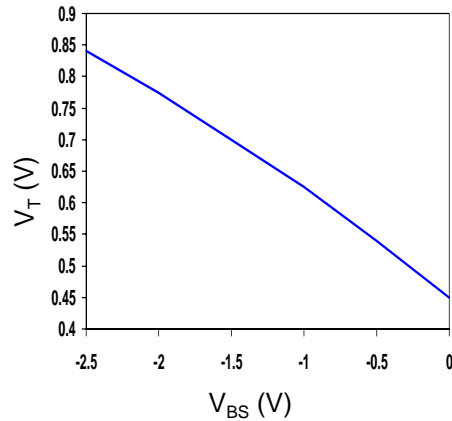
$\gamma = \sqrt{(2q\epsilon_{si}N_A)/C_{ox}}$  is the **body-effect coefficient** (impact of changes in  $V_{SB}$ ) ( $\epsilon_{si} = 1.053 \times 10^{-10} \text{ F/m}$  is the permittivity of silicon;  $C_{ox} = \epsilon_{ox}/t_{ox}$  is the gate oxide capacitance with  $\epsilon_{ox} = 3.5 \times 10^{-11} \text{ F/m}$ )

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## The Body Effect



- $V_{SB}$  is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes  $V_T$  to increase from 0.45V to 0.85V

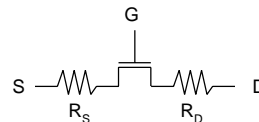
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## Other (Submicron) MOS Transistor Concerns

- **Velocity saturation**
- **Subthreshold conduction**
  - Transistor is already partially conducting for voltages below  $V_T$
- **Threshold variations**
  - In long-channel devices, the threshold is a function of the length (for low  $V_{DS}$ )
  - In short-channel devices, there is a drain-induced threshold barrier lowering at the upper end of the  $V_{DS}$  range (for low  $L$ )
- **Parasitic resistances**
  - resistances associated with the source and drain contacts
- **Latch-up**

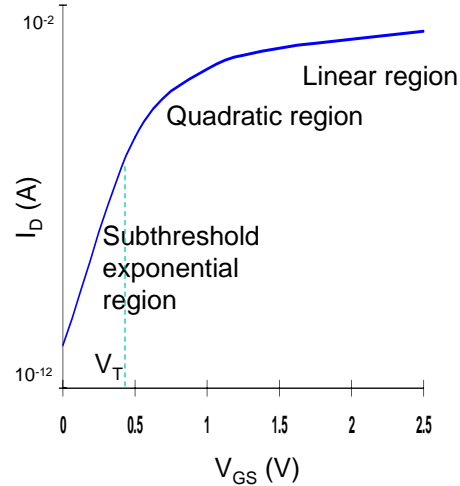


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## Subthreshold Conductance



- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature

$$S = n \left( \frac{kT}{q} \right) \ln(10)$$

(typical values 60 to 100 mV/decade)

- Has repercussions in dynamic circuits and for power consumption

$$I_D \sim I_S e^{(qV_{GS}/nkT)} \quad \text{where } n \geq 1$$

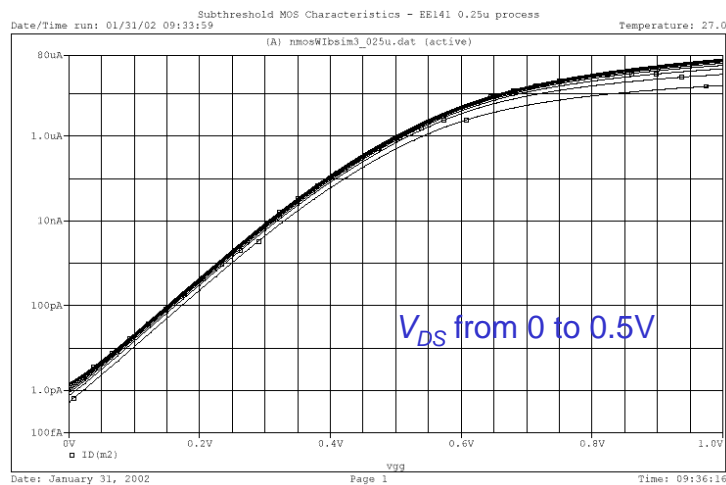
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## Subthreshold $I_D$ vs $V_{GS}$

$$I_D = I_S e^{(qV_{GS}/nkT)} (1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$



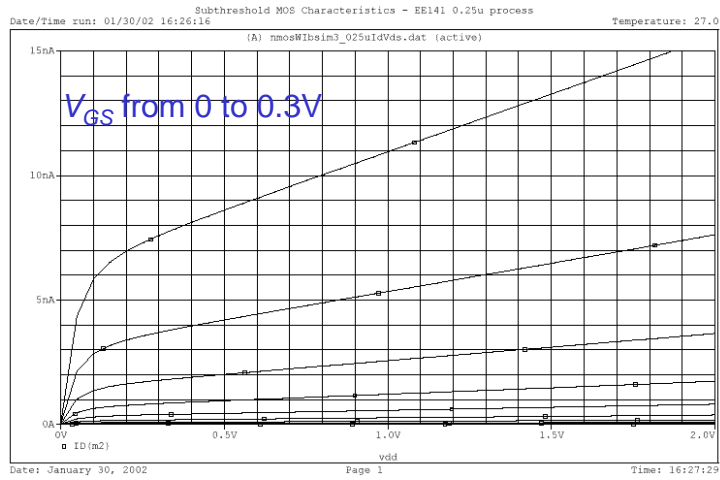
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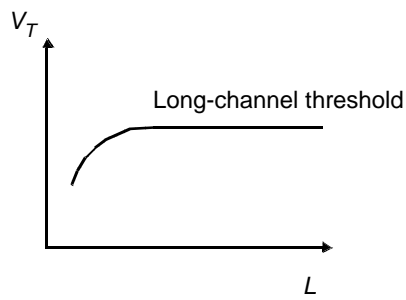
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## Subthreshold $I_D$ vs $V_{DS}$

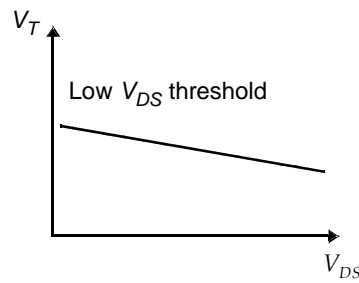
$$I_D = I_S e^{(qV_{GS}/nkT)} (1 - e^{-(qV_{DS}/kT)})(1 + \lambda V_{DS})$$



## Threshold Variations



Threshold as a function of the length (for low  $V_{DS}$ )



Drain-induced barrier lowering (for low  $L$ )

## Voltage-Current Relation: Linear Mode

For long-channel devices ( $L > 0.25$  micron)

- When  $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n W/L [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

where

$k'_n = \mu_n C_{ox} = \mu_n \epsilon_{ox} / t_{ox}$  is the **process transconductance parameter** ( $\mu_n$  is the carrier mobility ( $m^2/Vsec$ ))

$k_n = k'_n W/L$  is the **gain factor** of the device

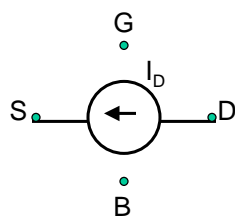
- For small  $V_{DS}$ , there is a linear dependence between  $V_{DS}$  and  $I_D$ , hence the name **resistive** or **linear** region

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## The MOS Current-Source Model



$$I_D = 0 \text{ for } V_{GS} - V_T \leq 0$$

$$I_D = k' W/L [(V_{GS} - V_T)V_{min} - V_{min}^2/2](1 + \lambda V_{DS})$$

for  $V_{GS} - V_T \geq 0$

with  $V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT})$   
and  $V_{GT} = V_{GS} - V_T$

- Determined by the voltages at the four terminals and a set of five device parameters

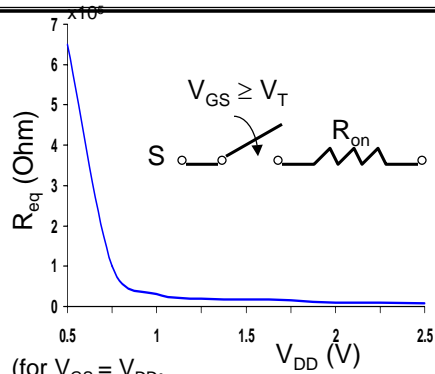
	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	$115 \times 10^{-6}$	0.06
PMOS	-0.4	-0.4	-1	$-30 \times 10^{-6}$	-0.1

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## The Transistor Modeled as a Switch



(for  $V_{GS} = V_{DD}$ ,  
 $V_{DS} = V_{DD} \rightarrow V_{DD}/2$ )

Modeled as a switch with infinite off resistance and a finite on resistance,  $R_{on}$

- Resistance inversely proportional to  $W/L$  (doubling  $W$  halves  $R_{on}$ )
- For  $V_{DD} \gg V_T + V_{DSAT}/2$ ,  $R_{on}$  independent of  $V_{DD}$
- Once  $V_{DD}$  approaches  $V_T$ ,  $R_{on}$  increases dramatically

$V_{DD}$ (V)	1	1.5	2	2.5
NMOS (k $\Omega$ )	35	19	15	13
PMOS (k $\Omega$ )	115	55	38	31

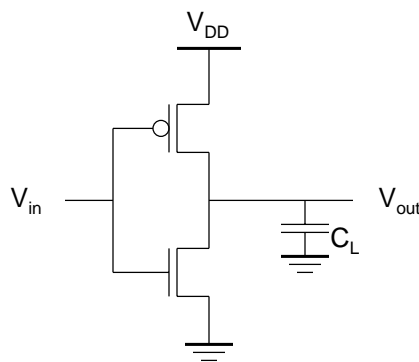
$R_{on}$  (for  $W/L = 1$ )  
 For larger devices  
 divide  $R_{eq}$  by  $W/L$

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## Next Time: The CMOS Inverter



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