CPE/EE 427, CPE 527
VLSI Design I
L04: MOS Transistors Theory

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Course Administration

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• Labs: Lab#1 this week

• Text: CMOS VLSI Design, 3rd ed., Weste, Harris

• Review: Introduction, Design Metrics, IC Fabrication
  (Read Chapter 1); IC Fabrication (Chapter 3)

• Today: MOS Transistor Theory (Chapter 2)
Review: Simplified CMOS Inverter Process

- cut line
- p well

Review: Intra-Layer Design Rules

- Same Potential
- Different Potential
  - Well
  - Active
  - Select
  - Polysilicon
  - Metal1
  - Metal2
  - Contact or Via Hole

9/6/2005 VLSI Design I; A. Milenkovic
Review: Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers
   - Transistors
   - Catastrophic error
   - Unrelated Poly & Diffusion
     - Thinner diffusion, but still working

Review: Vias and Contacts

- Via
- Metal to Poly Contact
- Metal to Active Contact
Outline

• Introduction
• MOS Capacitor
• nMOS I-V Characteristics
• pMOS I-V Characteristics
• Gate and Diffusion Capacitance
• Non-Ideal IV Effects

Introduction

• So far, we have treated transistors as ideal switches
• An ON transistor passes a finite amount of current
  – Depends on terminal voltages
  – Derive current-voltage (I-V) relationships
• Transistor gate, source, drain all have capacitance
  – I = C (∆V/∆t) -> ∆t = (C/I) ∆V
  – Capacitance and current determine speed
• Also explore what a “degraded level” really means
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion

![Diagrams](image)

Terminal Voltages

- Mode of operation depends on \( V_{g}, V_{d}, V_{s} \)
  - \( V_{gs} = V_{g} - V_{s} \)
  - \( V_{gd} = V_{g} - V_{d} \)
  - \( V_{ds} = V_{d} - V_{s} = V_{gs} - V_{gd} \)
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence \( V_{ds} \geq 0 \)
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - Cutoff
  - Linear
  - Saturation
nMOS Cutoff

- No channel
- \( I_{ds} = 0 \)

![nMOS Cutoff Diagram]

nMOS Linear

- Channel forms
- Current flows from d to s
  - \( e^- \) from s to d
- \( I_{ds} \) increases with \( V_{ds} \)
- Similar to linear resistor

![nMOS Linear Diagram]
nMOS Saturation

- Channel pinches off
- \( I_{ds} \) independent of \( V_{ds} \)
- We say current saturates
- Similar to current source

\[ V_{gs} > V_t \]
\[ V_{gd} < V_t \]
\[ V_{ds} > V_{gs} - V_t \]

p-type body

I-V Characteristics

- In Linear region, \( I_{ds} \) depends on
  - How much charge is in the channel?
  - How fast is the charge moving?
Channel Charge

• MOS structure looks like parallel plate capacitor while operating in inversion
  – Gate – oxide – channel
• $Q_{\text{channel}} = CV$
  • $C =$

[Diagram of MOS structure with labels for $V_{gs}, V_{gd}, V_{ds}, W, L, \text{SiO}_2$ gate oxide (good insulator, $\varepsilon_{\text{ox}} = 3.9$), polysilicon gate]
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C = C_g = \varepsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}}WL$
  \[ C_{\text{ox}} = \varepsilon_{\text{ox}} / t_{\text{ox}} \]
- $V =$

![MOS structure diagram]

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C = C_g = \varepsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}}WL$
  \[ C_{\text{ox}} = \varepsilon_{\text{ox}} / t_{\text{ox}} \]
- $V =$ $V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

![MOS structure diagram]
Carrier velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
- $v = \mu E$

$\mu$ called mobility

E =
Carrier velocity

• Charge is carried by e-
• Carrier velocity $v$ proportional to lateral E-field between source and drain
  - $v = \mu E$
  - $\mu$ called mobility
• $E = V_{ds}/L$
• Time for carrier to cross channel:
  - $t = \frac{L}{v}$
nMOS Linear I-V

• Now we know
  – How much charge $Q_{\text{channel}}$ is in the channel
  – How much time $t$ each carrier takes to cross

$$I_{ds} =$$
nMOS Linear I-V

Now we know
- How much charge $Q_{channel}$ is in the channel
- How much time $t$ each carrier takes to cross

$$I_{ds} = \frac{Q_{channel}}{t}$$

$$= \mu C_{ox} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$\beta = \mu C_{ox} \frac{W}{L}$

nMOS Saturation I-V

If $V_{gd} < V_t$, channel pinches off near drain
- When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} =$$
nMOS Saturation I-V

• If $V_{gd} < V_t$, channel pinches off near drain
  – When $V_{ds} > V_{dsat} = V_{gs} - V_t$
• Now drain voltage no longer increases current

$$I_{ds} = \beta \left(V_{gs} - V_t - \frac{V_{dsat}}{2}\right) V_{dsat}$$
nMOS I-V Summary

- **Shockley 1st order transistor models**

\[
I_{ds} = \begin{cases} 
0 & V_{gs} < V_t \quad \text{cutoff} \\
\beta \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\
\frac{\beta}{2} \left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation}
\end{cases}
\]

Example

- **For a 0.6 \( \mu \)m process**
  - From AMI Semiconductor
  - \( t_{ox} = 100 \) Å
  - \( \mu = 350 \) cm\(^2/V\cdot s\)
  - \( V_t = 0.7 \) V
- **Plot** \( I_{ds} \) vs. \( V_{ds} \)
  - \( V_{gs} = 0, 1, 2, 3, 4, 5 \)
  - Use \( W/L = 4/2 \) \( \lambda \)

\[
\beta = \mu C_{ox} \frac{W}{L} = (350) \left(3.9 \times 10^{-14} - \frac{1}{100 - 10^{-14}} \right) \left(\frac{W}{L}\right) = 120 \frac{W}{L} \mu A/V^2
\]
pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility $\mu_p$ is determined by holes
  - Typically 2-3x lower than that of electrons $\mu_n$
  - 120 cm$^2$/V*s in AMI 0.6 um process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$
  - *** plot I-V here

Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion
Gate Capacitance (simple model)

- Approximate channel as connected to source
- \( C_{gs} = \varepsilon_{ox} \frac{W}{t_{ox}} = C_{ox} \frac{W}{L} = C_{permicron} W \)
- \( C_{permicron} \) is typically about 2 fF/μm

![Diagram of gate capacitance](image)

Diffusion Capacitance (simple model)

- \( C_{sb}, C_{db} \)
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to \( C_g \) for contacted diff
  - \( \frac{1}{2} C_g \) for uncontacted
  - Varies with process
MOS Structure Capacitances

Overlapping capacitance (linear)

\[ C_{GSO} = C_{GDO} = C_{ox} x_d W = C_o W \]

MOS Channel Capacitances

- The gate-to-channel capacitance depends upon the operating region and the terminal voltages

\[ C_{GS} = C_{GCS} + C_{GSO} \quad C_{GD} = C_{GCD} + C_{GDO} \]
Average Distribution of Channel Capacitance

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>( C_{GB} )</th>
<th>( C_{GS} )</th>
<th>( C_{GD} )</th>
<th>( C_G )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>( C_{ox, WL} )</td>
<td>0</td>
<td>0</td>
<td>( C_{ox, WL} ) + ( 2C_{ox, WL} )</td>
</tr>
<tr>
<td>Resistive</td>
<td>0</td>
<td>( C_{ox, WL/2} )</td>
<td>( C_{ox, WL/2} )</td>
<td>( C_{ox, WL} ) + ( 2C_{ox, WL} )</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>( (2/3)C_{ox, WL} )</td>
<td>0</td>
<td>( (2/3)C_{ox, WL} ) + ( 2C_{ox, WL} )</td>
</tr>
</tbody>
</table>

- Channel capacitance components are nonlinear and vary with operating voltage
- Most important regions are cutoff and saturation since that is where the device spends most of its time

MOS Diffusion Capacitances

- The junction (or diffusion) capacitance is from the reverse-biased source-body and drain-body pn-junctions.

\[
C_{SB} = C_{Sdiff} \quad \text{and} \quad C_{DB} = C_{Ddiff}
\]
Source Junction View

\[ C_{\text{diff}} = C_{\text{bp}} + C_{\text{sw}} = C_j \text{AREA} + C_{jsw} \text{PERIMETER} \]
\[ = C_j L_S W + C_{jsw} (2L_S + W) \]

Recap: The Diode

Cross-section of \(pn\)-junction in an IC process

One-dimensional representation

diode symbol

 Mostly occurring as parasitic element in Digital ICs
Recap: Depletion Region

(a) Current flow.
(b) Charge density.
(c) Electric field.
(d) Electrostatic potential.

Recap: Diode Current

\[
I_D = I_S \left(e^{V_D/T} - 1\right)
\]
Recap: Ideal Diode Equation

- The *ideal diode equation* (for both forward and reverse-bias conditions) is
  \[ I_D = I_S (e^{V_D/\phi_T} - 1) \]

where \( V_D \) is the voltage applied to the junction
- a forward-bias lowers the potential barrier allowing carriers to flow across the diode junction
- a reverse-bias raises the potential barrier and the diode becomes nonconducting

\[ \phi_T = kT/q = 26\text{mV at 300K} \]

\( I_S \) is the saturation current of the diode

\[ V_D \quad \text{mV} \]

\[ I_D \quad \text{mA} \]

MOS Diffusion Capacitances

\[ C_{\text{diff}} = C_{\text{bp}} + C_{\text{sw}} = C_{\text{bp}} \text{AREA} + C_{\text{sw}} \text{PERIMETER} \]

= \[ C_{\text{bp}} L_S W + C_{\text{sw}} (2L_S + W) \]

Source parasitic:

\[ C_{\text{jbs}} = C_J (1 + V_{sb}/\psi_0)^{Mj} \]

- \( C_J \) – junction capacitance at zero bias
- \( Mj \) – junction grading coefficient (0.5 – 0.33)
- \( \psi_0 = \nu_T \ln(N_A N_D / n_i^2) \)

\[ C_{\text{jbsw}} = C_{\text{JSW}} (1 + V_{sb}/\psi_0)^{Mjsw} \]

- \( C_{\text{JSW}} \) – junction capacitance at zero bias
- \( Mjsw \) – junction grading coefficient (0.5 – 0.33)
MOS Capacitance Model

\[
\begin{align*}
C_{GS} &= C_{GCS} + C_{GSO} \\
C_{GD} &= C_{GCD} + C_{GDO} \\
C_{SB} &= C_{Sdiff} \\
C_{GB} &= C_{GCB} \\
C_{DB} &= C_{Ddiff}
\end{align*}
\]

Transistor Capacitance Values for 0.25 \(\mu\)m

Example: For an NMOS with \(L = 0.24\ \mu\)m, \(W = 0.36\ \mu\)m, \(L_D = L_S = 0.625\ \mu\)m
\[
\begin{align*}
C_{GSO} &= C_{GDO} = C_{ox} x_d W = C_{o} W \\
C_{GC} &= C_{ox} WL \\
so\ C_{gate\_cap} &= C_{ox} WL + 2C_{o}W = \\
C_{bp} &= C_{j} L_S W = \\
C_{sw} &= C_{jsw} (2L_S + W) = \\
so\ C_{diffusion\_cap} &= 
\end{align*}
\]

<table>
<thead>
<tr>
<th></th>
<th>(C_{ox}) (fF/\mu m^2)</th>
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<th>(m_j)</th>
<th>(\phi_b) (V)</th>
<th>(C_{jsw}) (fF/\mu m)</th>
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<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
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<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
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Transistor Capacitance Values for 0.25 μm

Example: For an NMOS with \( L = 0.24 \, \mu m \), \( W = 0.36 \, \mu m \),

\[ L_D = L_S = 0.625 \, \mu m \]

\[ C_{GSO} = C_{GDO} = C_{ox} \times_d W = C_o \times W = 0.11 \, fF \]

\[ C_{GC} = C_{ox} \times WL = 0.52 \, fF \]

so \( C_{gate\_cap} = C_{ox} \times WL + 2C_o \times W = 0.74 \, fF \)

\[ C_{bp} = C_j \times L_S \times W = 0.45 \, fF \]

\[ C_{sw} = C_{jsw} \times (2L_S + W) = 0.45 \, fF \]

so \( C_{diffusion\_cap} = 0.90 \, fF \)

<table>
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<tr>
<th></th>
<th>( C_{ox} ) (fF/μm²)</th>
<th>( C_o ) (fF/μm)</th>
<th>( C_j ) (fF/μm²)</th>
<th>( m_j )</th>
<th>( \phi_b ) (V)</th>
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Non-Ideal I-V Effects

- \( I_{ds\_sat} \) increases less than quadratically with increasing \( V_{gs} \)
  - Velocity saturation & mobility degradation
  \[ I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{dr} & V_{dr} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} \left(V_{gs} - V_t\right)^2 & V_{dr} > V_{dsat} \quad \text{saturation} \end{cases} \]
- \( I_{ds\_sat} \) increases slightly with \( V_{ds} \)
  - Channel length modulation
- \( V_T \) is influenced by the \( V_{sb} \)
  - Body effect
- There is current flow in nominally OFF transistors
  - Subthreshold conduction (junction leakage, tunnel)
Current Determinates

- For a fixed $V_{DS}$ and $V_{GS} (> V_T)$, $I_{DS}$ is a function of
  - the distance between the source and drain – $L$
  - the channel width – $W$
  - the threshold voltage – $V_T$
  - the thickness of the SiO₂ – $t_{ox}$
  - the dielectric of the gate insulator (SiO₂) – $\varepsilon_{ox}$
  - the carrier mobility
    - for nfets: $\mu_n = 500 \, \text{cm}^2/\text{V}-\text{sec}$
    - for pfets: $\mu_p = 180 \, \text{cm}^2/\text{V}-\text{sec}$

Long Channel I-V Plot (NMOS)

NMOS transistor, 0.25um, $L_d = 10\, \mu$m, $W/L = 1.5$, $V_{DD} = 2.5V$, $V_T = 0.4V$
Short Channel Effects

- Behavior of short channel device mainly due to
  \( \nu_{\text{sat}} = 10^5 \)

- Velocity saturation — the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

- For an NMOS device with \( L \) of .25\( \mu \)m, only a couple of volts difference between \( D \) and \( S \) are needed to reach velocity saturation

Voltage-Current Relation: Velocity Saturation

For short channel devices

- Linear: When \( V_{DS} \leq V_{GS} - V_T \)
  \[ I_D = \kappa(V_{DS}) k'_n \frac{W}{L} [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \]
  where
  \[ \kappa(V) = \frac{1}{1 + (V/\xi_c L)} \] is a measure of the degree of velocity saturation

- Saturation: When \( V_{DS} = V_{DSAT} \geq V_{GS} - V_T \)
  \[ I_{DSat} = \kappa(V_{DSAT}) k'_n \frac{W}{L} [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2] \]
Velocity Saturation Effects

- For short channel devices and large enough $V_{GS} - V_T$:
  - $V_{DSAT} < V_{GS} - V_T$ so the device enters saturation before $V_{DS}$ reaches $V_{GS} - V_T$ and operates more often in saturation.

- $I_{DSAT}$ has a linear dependence wrt $V_{GS}$ so a reduced amount of current is delivered for a given control voltage.

Short Channel I-V Plot (NMOS)

- NMOS transistor, $0.25 \mu m$, $L_d = 0.25 \mu m$, $W/L = 1.5$, $V_{DD} = 2.5V$, $V_T = 0.4V$.
MOS $I_D$-$V_{GS}$ Characteristics

- Linear (short-channel) versus quadratic (long-channel) dependence of $I_D$ on $V_{GS}$ in saturation

- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of $V_{DS}$ resulting in a substantial drop in current drive

(for $V_{DS} = 2.5V$, $W/L = 1.5$)

Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed

PMOS transistor, $0.25\mu m$, $L_d = 0.25\mu m$, $W/L = 1.5$, $V_{DD} = 2.5V$, $V_T = -0.4V$
Transistor in Saturation Mode

Assuming $V_{GS} > V_T$

The current remains constant (saturates).

Voltage-Current Relation: Saturation Mode

For long channel devices

- When $V_{DS} \geq V_{GS} - V_T$
  \[ I_D' = \frac{k'}{2} \frac{W}{L} [(V_{GS} - V_T)^2] \]

  since the voltage difference over the induced channel (from the pinch-off point to the source) remains fixed at $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied $V_{DS}$, so
  \[ I_D = I_D' (1 + \lambda V_{DS}) \]

  where $\lambda$ is the channel-length modulation (varies with the inverse of the channel length)
Threshold Voltage Concept

The value of $V_{GS}$ where strong inversion occurs is called the threshold voltage, $V_T$.

The Threshold Voltage

\[ V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \]

where

- $V_{T0}$ is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process
  - Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.
- $V_{SB}$ is the source-bulk voltage
- $\phi_F = -\phi_T \ln (N_A/n_i)$ is the Fermi potential ($\phi_T = kT/q = 26mV$ at 300K is the thermal voltage; $N_A$ is the acceptor ion concentration; $n_i \approx 1.5x10^{10}$ cm$^{-3}$ at 300K is the intrinsic carrier concentration in pure silicon)
- $\gamma = \sqrt{2q\varepsilon_s N_A}/C_{ox}$ is the body-effect coefficient (impact of changes in $V_{SB}$) ($\varepsilon_s = 1.053x10^{-13}$F/m is the permittivity of silicon; $C_{ox} = \varepsilon_0 / t_{ox}$ is the gate oxide capacitance with $\varepsilon_0 = 3.5x10^{-13}$F/m)
The Body Effect

- $V_{SB}$ is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground).
- A negative bias causes $V_T$ to increase from 0.45V to 0.85V.

Other (Submicon) MOS Transistor Concerns

- Velocity saturation
- Subthreshold conduction
  - Transistor is already partially conducting for voltages below $V_T$.
- Threshold variations
  - In long-channel devices, the threshold is a function of the length (for low VDS).
  - In short-channel devices, there is a drain-induced threshold barrier lowering at the upper end of the VDS range (for low L).
- Parasitic resistances
  - Resistances associated with the source and drain contacts.
- Latch-up
Subthreshold Conductance

- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature

\[ S = n \frac{(kT)}{q} \ln(10) \] (typical values 60 to 100 mV/decade)

- Has repercussions in dynamic circuits and for power consumption

Subthreshold \( I_D \) vs \( V_{GS} \)

\[ I_D = I_S e^{\left(\frac{qV_{GS}}{nkT}\right)} \left(1 - e^{-\left(\frac{qV_D}{kT}\right)}\right) \left(1 + \lambda V_D\right) \]
**Subthreshold $I_D$ vs $V_{DS}$**

$$I_D = I_S \, e^{(qV_{GS}/nkT)} \left( 1 - e^{-(qV_{DS}/kT)} \right) \left( 1 + \lambda V_{DS} \right)$$

**Threshold Variations**

- **Long-channel threshold**
- **Low $V_{DS}$ threshold**
- **Drain-induced barrier lowering**

Threshold as a function of the length (for low $V_{DS}$)

Drain-induced barrier lowering (for low $L$)
Voltage-Current Relation: Linear Mode

For long-channel devices (L > 0.25 micron)

- When $V_{DS} \leq V_{GS} - V_T$

\[
I_D = k'_n \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - V_{DS}^2 / 2 \right]
\]

where

\[
k'_n = \mu_n C_{ox} = \mu_n \frac{C_{ox}}{t_{ox}} = \text{is the process transconductance parameter (}\mu_n\text{ is the carrier mobility (m}^2/\text{Vsec))}
\]

$k_n = k'_n \frac{W}{L}$ is the gain factor of the device

- For small $V_{DS}$, there is a linear dependence between $V_{DS}$ and $I_D$, hence the name resistive or linear region

The MOS Current-Source Model

\[
I_D = 0 \text{ for } V_{GS} - V_T \leq 0
\]

\[
I_D = k' \frac{W}{L} \left[ (V_{GS} - V_T) V_{min} - V_{min}^2 / 2 \right] (1 + \lambda V_{DS})
\]

for $V_{GS} - V_T \geq 0$

with $V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT})$

and $V_{GT} = V_{GS} - V_T$

- Determined by the voltages at the four terminals and a set of five device parameters

<table>
<thead>
<tr>
<th></th>
<th>$V_{TO}(V)$</th>
<th>$\gamma(V^{0.5})$</th>
<th>$V_{DSAT}(V)$</th>
<th>$k'(A/V^2)$</th>
<th>$\lambda(V^{-1})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>$115 \times 10^{-6}$</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>$-30 \times 10^{-6}$</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

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The Transistor Modeled as a Switch

Modeled as a switch with infinite off resistance and a finite on resistance, $R_{on}$

- Resistance inversely proportional to $W/L$ (doubling $W$ halves $R_{on}$)
- For $V_{DD} >> V_T + V_{DSAT}/2$, $R_{on}$ independent of $V_{DD}$
- Once $V_{DD}$ approaches $V_T$, $R_{on}$ increases dramatically

<table>
<thead>
<tr>
<th>$V_{DD}$ (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

For larger devices divide $R_{eq}$ by $W/L$

Next Time: The CMOS Inverter