Review: CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
  - full rail-to-rail swing
  - $V_{OH}$ and $V_{OL}$ are at VDD and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between VDD and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)

- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

Review: Static Complementary CMOS

Pull-up network (PUN) and pull-down network (PDN)

PMOS transistors only
- pull-up: make a connection from VDD to $F$ when $F(I_{n1}, I_{n2}, \ldots, I_{nN}) = 1$
- pull-down: make a connection from $F$ to GND when $F(I_{n1}, I_{n2}, \ldots, I_{nN}) = 0$
NMOS transistors only

PUN and PDN are dual logic networks

What logic function is this?

AOI221

OAI21 Logic Graph
Two Stick Layouts of \( !(C \cdot (A + B)) \)

![Diagram of two stick layouts](image)

Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph.
- Euler path: a path through all nodes in the graph such that each edge is visited once and only once.
- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same).

![Diagram of consistent Euler path](image)

Consistent Euler Path

![Diagram of OAI22 logic graph](image)

OAI22 Logic Graph

![Diagram of OAI22 layout](image)

Combinational Logic Cells (cont’d)

- The AOI family of cells with 3 index numbers or less:
  - \( X = \{\text{AOI, OAI, AO, OA}\}; a, b, c = \{2, 3\} \)

<table>
<thead>
<tr>
<th>Cell Type</th>
<th>Cells</th>
<th>Number of Unique Cells</th>
</tr>
</thead>
<tbody>
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<td>Xa1</td>
<td>X21, X31</td>
<td>2</td>
</tr>
<tr>
<td>Xa11</td>
<td>X211, X311</td>
<td>2</td>
</tr>
<tr>
<td>Xab</td>
<td>X22, X33, X32</td>
<td>3</td>
</tr>
<tr>
<td>Xabc</td>
<td>X221, X321, X332, X322</td>
<td>4</td>
</tr>
<tr>
<td>Total</td>
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<td>14</td>
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</tbody>
</table>
VTC is Data-Dependent

\[ V_{ds} = V_{ds1} - V_{ds2} \]

- The threshold voltage of \( M_2 \) is higher than \( M_1 \) due to the body effect (\( \gamma \))

\[ V_{Tn2} = V_{Tn0} + \gamma (\sqrt{|2\phi_F| + V_{int}} - \sqrt{|2\phi_F|}) \]

since \( V_{ds} \) of \( M_2 \) is not zero (when \( V_g = 0 \)) due to the presence of \( C_{int} \)

\[ V_{G1} = V_B \]

\[ V_{G2} = V_A - V_{DS1} \]

\[ F = A \land B \]

\[ AB \]

\[ M1 \]

\[ M2 \]

\[ M3 \]

\[ M4 \]

\[ C \]

\[ int \]

\[ \text{Static CMOS Full Adder Circuit} \]

\[ \neg C_{out} = \neg C_{in} \land (\neg A \land \neg B) \lor (\neg A \land \neg B) \]

\[ C_{out} = C_{in} \land (A \lor B) \lor (A \land B) \]

\[ \neg \text{Sum} = C_{out} \land (\neg A \land \neg B \land \neg C_{in}) \lor (\neg A \land \neg B \land \neg C_{in}) \]

\[ \text{Sum} = \neg C_{out} \land (A \lor B \lor C_{in}) \lor (A \land B \land C_{in}) \]

\[ \text{Pass Transistor Logic} \]

\[ \text{NMOS Transistors in Series/Parallel} \]

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high

\[ X = Y \text{ if } A \text{ and } B \]

\[ X = Y \text{ if } A \text{ or } B \]

- Remember – NMOS transistors pass a strong 0 but a weak 1

\[ \text{PMOS Transistors in Series/Parallel} \]

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low

\[ X = Y \text{ if } \overline{A} \text{ and } B = A + B \]

\[ X = Y \text{ if } \overline{A} \text{ or } B = A \cdot B \]

- Remember – PMOS transistors pass a strong 1 but a weak 0
Pass Transistor (PT) Logic

- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus unidirectional)

VTC of PT AND Gate

Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

Differential PT Logic (CPL)

- Differential so complementary data inputs and outputs are always available (so don’t need extra inverters)
- Still static, since the output defining nodes are always tied to VDD or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

CPL Full Adder

CPL Full Adder
**NMOS Only PT Driving an Inverter**

- $V_x$ does not pull up to $V_{DD}$, but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power consumption ($M$, may be weakly conducting forming a path from $V_{DD}$ to GND)
- Notice $V_x$ increases of pass transistor due to body effect ($V_{gs}$)

**Voltage Swing of PT Driving an Inverter**

- Body effect – large $V_{gs}$ at $x$ - when pulling high ($B$ is tied to GND and S charged up close to $V_{DD}$)
- So the voltage drop is even worse

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{|2\phi_f| + V_x} - \sqrt{|2\phi_f|}))$$

**Cascaded NMOS Only PTs**

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

**Solution 1: Level Restorer**

- Full swing on $x$ (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when $A$ is high
- For correct operation $M_r$ must be sized correctly (ratioed)

**Solution 2: Multiple $V_T$ Transistors**

- Technology solution: Use (near) zero $V_T$ devices for the NMOS PTs to eliminate most of the threshold drop (body effect still in force preventing full swing to $V_{DD}$)
- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if $V_{gs}$ is below $V_{Tn}$)

**Transient Level Restorer Circuit Response**

- Restorer has speed and power impacts: increases the capacitance at $x$, slowing down the gate; increases $t$, (but decreases $t_f$)
Solution 3: Transmission Gates (TGs)

- Most widely used solution

![Diagram of TGs]

- Full swing bidirectional switch controlled by the gate signal $C$, $A = B$ if $C = 1$

Resistance of TG

![Graph showing resistance vs. voltage]

TG Multiplexer

![Diagram of TG multiplexer]

Transmission Gate XOR

![Diagram of XOR gate]

Transmission Gate XOR

![Diagram of XOR gate with explanation of weak 0 and weak 1]

$F = \overline{\left(I_n \cdot S + I_n \cdot \overline{S}\right)}$
### TG Full Adder

<table>
<thead>
<tr>
<th>( A )</th>
<th>( B )</th>
<th>( C_{in} )</th>
<th>Sum</th>
<th>( C_{out} )</th>
</tr>
</thead>
</table>

### Differential TG Logic (DPL)

<table>
<thead>
<tr>
<th>( A )</th>
<th>( B )</th>
<th>( C_{in} )</th>
<th>( V_{dd} )</th>
<th>( V_{ss} )</th>
</tr>
</thead>
</table>

**Logic Gates**

- **AND/NAND**
  - \( F = A \oplus B \)
- **XOR/XNOR**
  - \( F = AB \)