Review: CMOS Circuit Styles

- **Static complementary CMOS** - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
  - full rail to rail swing
  - VOH and VOL are at VDD and GND, respectively
- low output impedance, high input impedance
- no steady state path between VDD and GND (no static power consumption)
- delay a function of load capacitance and transistor resistance
- comparable rise and fall times (under the appropriate transistor sizing conditions)

- **Dynamic CMOS** - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise
Review: Static Complementary CMOS

Pull-up network (PUN) and pull-down network (PDN)

PMOS transistors only

pull-up: make a connection from $V_{DD}$ to $F$ when $F(In_1, In_2, \ldots, In_N) = 1$

NMOS transistors only

pull-down: make a connection from $F$ to GND when $F(In_1, In_2, \ldots, In_N) = 0$

PUN and PDN are dual logic networks

AOI221

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PUN and PDN are dual logic networks

AOI221
What logic function is this?

OAI21 Logic Graph

\[
X = \overline{C \cdot (A + B)}
\]
Two Stick Layouts of \( !(C \cdot (A + B)) \)

![Diagram showing two stick layouts of \( !(C \cdot (A + B)) \)](image-url)

An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph:

- Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

**Consistent Euler Path**

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph.
- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be **consistent** (the same).
**Consistent Euler Path**

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be **consistent** (the same)

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**OAI22 Logic Graph**

- \[ X = \neg ((A+B) \cdot (C+D)) \]
Some functions have no consistent Euler path like $x = !(a + bc + de)$ (but $x = !(bc + a + de)$ does!)

### Combinational Logic Cells (cont’d)

- The AOI family of cells with 3 index numbers or less
  - $X = \{AOI, OAI, AO, OA\}; a,b,c=\{2,3\}$

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<th>Number of Unique Cells</th>
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<tr>
<td><strong>Total</strong></td>
<td><strong>14</strong></td>
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VTC is Data-Dependent

- The threshold voltage of $M_2$ is higher than $M_1$ due to the body effect ($\gamma$)

\[
V_{Tn1} = V_{Tn0} \\
V_{Tn2} = V_{Tn0} + \gamma(\sqrt{2\phi_F} + V_{int}) - \sqrt{2\phi_F}
\]

since $V_{SB}$ of $M_2$ is not zero (when $V_B = 0$) due to the presence of $C_{int}$

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Static CMOS Full Adder Circuit

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**Static CMOS Full Adder Circuit**

\[
\begin{align*}
!C_{out} &= !C_{in} \land (A \lor !B) \lor (A \land !B) \\
!Sum &= C_{out} \land (A \lor !B \lor !C_{in}) \lor (A \land !B \land !C_{in}) \\
C_{out} &= C_{in} \land (A \lor B) \lor (A \land B) \\
Sum &= !C_{out} \land (A \lor B \lor C_{in}) \lor (A \land B \land C_{in})
\end{align*}
\]

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**Pass Transistor Logic**
**NMOS Transistors in Series/Parallel**

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high

\[
\begin{align*}
X = Y & \text{ if } A \text{ and } B \\
X = Y & \text{ if } A \text{ or } B
\end{align*}
\]

- Remember –
  NMOS transistors pass a strong 0 but a weak 1

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**PMOS Transistors in Series/Parallel**

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low

\[
\begin{align*}
X = Y & \text{ if } \overline{A} \text{ and } \overline{B} = A + B \\
X = Y & \text{ if } \overline{A} \text{ or } \overline{B} = A \cdot B
\end{align*}
\]

- Remember –
  PMOS transistors pass a strong 1 but a weak 0
Pass Transistor (PT) Logic

- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)

VTC of PT AND Gate

Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)
### Differential PT Logic (CPL)

![CPL Diagram]

### CPL Properties

- **Differential** so complementary data inputs and outputs are always available (so don’t need extra inverters)
- Still static, since the output defining nodes are always tied to $V_{DD}$ or GND through a low resistance path
- Design is **modular**; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like **adders**
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems
NMOS Only PT Driving an Inverter

- $V_x$ does not pull up to $V_{DD}$, but $V_{DD} - V_{Th}$
- Threshold voltage drop causes static power consumption ($M_2$ may be weakly conducting forming a path from $V_{DD}$ to GND)
- Notice $V_{Th}$ increases of pass transistor due to body effect ($V_{SB}$)

Voltage Swing of PT Driving an Inverter

- Body effect – large $V_{SB}$ at $x$ - when pulling high (B is tied to GND and S charged up close to $V_{DD}$)
- So the voltage drop is even worse
  \[ V_x = V_{DD} - (V_{Th}0 + \gamma(\sqrt{2\phi_I} + V_x) - \sqrt{2\phi_I}) \]
Cascaded NMOS Only PTs

Swing on \( y = V_{DD} - V_{Tn1} - V_{Tn2} \)

- Pass transistor gates should **never** be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

Solution 1: Level Restorer

- Full swing on \( x \) (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when \( A \) is high
- For correct operation \( M_r \) must be sized correctly (ratioed)
Transistor Level Restorer Circuit Response

- Restorer has speed and power impacts: increases the capacitance at x, slowing down the gate; increases t\textsubscript{l} (but decreases t\textsubscript{f})

Solution 2: Multiple V\textsubscript{T} Transistors

- Technology solution: Use (near) zero V\textsubscript{T} devices for the NMOS PTs to eliminate most of the threshold drop (body effect still in force preventing full swing to V\textsubscript{DD})

- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if V\textsubscript{GS} is below V\textsubscript{T})
Solution 3: Transmission Gates (TGs)

- Most widely used solution

- Full swing bidirectional switch controlled by the gate signal $C$, $A = B$ if $C = 1$
Resistance of TG

\[
\text{Resistance, } \Omega \quad \begin{array}{c}
0 & 5 & 10 & 15 & 20 & 25 & 30 \\
V_{\text{out}}, \text{V}
\end{array}
\]

\[
R_p \quad R_n \quad R_{eq}
\]

TG Multiplexer

\[F = !((In_1 \cdot S + In_2 \cdot \overline{S}))\]
Transmission Gate XOR

A ⊕ B

Transmission Gate XOR

weak 0 if !A
weak 1 if A

A • !B
B • !A

an inverter
TG Full Adder

Differential TG Logic (DPL)