CMOS Inverter: 
A First Look
CMOS Inverter: Steady State Response

\[ V_{DL} = 0 \]
\[ V_{OH} = V_{DD} \]
\[ V_M = f(R_n, R_p) \]

\[ V_{out} = 1 \quad V_{in} = V_{DD} \]
\[ V_{out} = 0 \quad V_{in} = 0 \]

CMOS Properties

- Full rail-to-rail swing \( \Rightarrow \) high noise margins
  - Logic levels not dependent upon the relative device sizes \( \Rightarrow \) transistors can be minimum size \( \Rightarrow \) ratioless
- Always a path to \( V_{dd} \) or GND in steady state \( \Rightarrow \) low output impedance (output resistance in kΩ range) \( \Rightarrow \) large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) \( \Rightarrow \) nearly zero steady-state input current
- No direct path steady-state between power and ground \( \Rightarrow \) no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors
Short Channel I-V Plot (NMOS)

NMOS transistor, 0.25um, $L_d = 0.25\text{um}$, $W/L = 1.5$, $V_D = 2.5V$, $V_T = 0.4V$

Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed

PMOS transistor, 0.25um, $L_d = 0.25\text{um}$, $W/L = 1.5$, $V_D = 2.5V$, $V_T = -0.4V$
nMOS Operation

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<tr>
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<th>Saturated</th>
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\[
\begin{align*}
V_{in} & \rightarrow V_{dd} \\
V_{out} & \rightarrow I_{ds} \\
V_{dsn} & \rightarrow I_{dsn}
\end{align*}
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### Saturated/Linear/Cutoff

- **Saturated**:
  - $V_{dsn} = V_{out}$
  - $V_{gsn} = V_{in}$

- **Linear**:  
  - $V_{dsn} > V_{gsn} - V_{tn}$
  - $V_{out} > V_{in} - V_{tn}$

- **Cutoff**:  
  - $V_{gsn} < V_{tn}$
  - $V_{in} < V_{tn}$

\[ V_{gsn} = V_{in} \]
\[ V_{dsn} = V_{out} \]
pMOS Operation

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Saturated: $Idsp < V_{out}$
Linear: $V_{in} < V_{gsp} - V_{tp}$

9/11/2006 VLSI Design I; A. Milenkovic

pMOS Operation

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Saturated: $Idsp < V_{out}$
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I-V Characteristics

• Make pMOS is wider than nMOS such that $\beta_n = \beta_p$

Current vs. $V_{out}, V_{in}$
Load Line Analysis

\( V_{in} = 0 \)

\[ \begin{align*}
V_{in0} \\
I_{dsn}, |I_{dspl}| \\
V_{DD} \\
\end{align*} \]

Load Line Analysis

\( V_{in} = 0.2V_{DD} \)

\[ \begin{align*}
V_{in1} \\
I_{dsn}, |I_{dspl}| \\
V_{DD} \\
\end{align*} \]
Load Line Analysis

• $V_{in} = 0.4V_{DD}$

Load Line Analysis

• $V_{in} = 0.6V_{DD}$
Load Line Analysis

- $V_{in} = 0.8V_{DD}$

Load Line Analysis

- $V_{in} = V_{DD}$
Load Line Summary

DC Transfer Curve

- Transcribe points onto $V_{in}$ vs. $V_{out}$ plot
CMOS Inverter Load Lines

\[ \text{PMOS} \quad \text{NMOS} \]

\[ \begin{align*}
V_{\text{in}} &= 0V \\
V_{\text{in}} &= 0.5V \\
V_{\text{in}} &= 1.0V \\
V_{\text{in}} &= 1.5V \\
V_{\text{in}} &= 2.0V \\
V_{\text{in}} &= 2.5V
\end{align*} \]

\[ \begin{align*}
V_{\text{out}} &= 0V \\
V_{\text{out}} &= 0.5V \\
V_{\text{out}} &= 1V \\
V_{\text{out}} &= 1.5V \\
V_{\text{out}} &= 2V \\
V_{\text{out}} &= 2.5V
\end{align*} \]

\[ 0.25\mu m, W/L_n = 1.5, W/L_p = 4.5, V_{DD} = 2.5V, V_{Tn} = 0.4V, V_{Tp} = -0.4V \]

CMOS Inverter VTC

\[ \begin{align*}
V_{\text{out}} (\text{V}) &= 0 \quad 0.5 \quad 1 \quad 1.5 \quad 2 \quad 2.5 \\
V_{\text{in}} (\text{V}) &= 0 \quad 0.5 \quad 1 \quad 1.5 \quad 2 \quad 2.5
\end{align*} \]
Operating Regions

- Revisit transistor operating regions

<table>
<thead>
<tr>
<th>Region</th>
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<th>pMOS</th>
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<td></td>
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CMOS Inverter VTC

- NMOS off
- PMOS res
- NMOS sat
- PMOS sat
- NMOS res
- PMOS off
**Beta Ratio**

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed gate*
- Other gates: collapse into equivalent inverter

**Noise Margins**

- How much noise can a gate input see before it does not recognize the input?
Logic Levels

- To maximize noise margins, select logic levels at
  - unity gain point of DC transfer characteristic
CMOS Inverter: Switch Model of Dynamic Behavior

Gate response time is determined by the time to charge $C_L$ through $R_p$ (discharge $C_L$ through $R_n$).
Relative Transistor Sizing

- When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS section to
  - maximize the noise margins and
  - obtain symmetrical characteristics

Switching Threshold

- $V_M$ where $V_{in} = V_{out}$ (both PMOS and NMOS in saturation since $V_{DS} = V_{GS}$)
  
  $V_M \approx rV_{DD}/(1 + r)$ where $r = k_p V_{DSATp}/k_n V_{DSATn}$

- Switching threshold set by the ratio $r$, which compares the relative driving strengths of the PMOS and NMOS transistors

- Want $V_M = V_{DD}/2$ (to have comparable high and low noise margins), so want $r \approx 1$

\[
\frac{(W/L)_p}{(W/L)_n} = \frac{k_n V_{DSATn}(V_{M} - V_{Tn} - V_{DSATn}/2)}{k_p V_{DSATp}(V_{DD} - V_{M} + V_{Tp} + V_{DSATp}/2)}
\]
Switch Threshold Example

• In our generic 0.25 micron CMOS process, using the process parameters from slide L03.25, a $V_{DD} = 2.5V$, and a minimum size NMOS device ((W/L)$_n$ of 1.5)

\[
\begin{array}{cccccc}
\text{NMOS} & V_{T0}(V) & \gamma(V^{0.5}) & V_{DSAT}(V) & k'(A/V^2) & \lambda(V^{-1}) \\
0.43 & 0.4 & 0.63 & 115 \times 10^{-6} & 0.06 \\
\text{PMOS} & -0.4 & -0.4 & -1 & -30 \times 10^{-6} & -0.1 \\
\end{array}
\]

\[
\frac{(W/L)_p}{(W/L)_n} = \frac{V_{T0}(V)}{V_{T0}(V)} \frac{\gamma(V^{0.5})}{\gamma(V^{0.5})} \frac{V_{DSAT}(V)}{V_{DSAT}(V)} \frac{k'(A/V^2)}{k'(A/V^2)} \frac{\lambda(V^{-1})}{\lambda(V^{-1})}
\]

\[
(W/L)_p = \frac{115 \times 10^{-6}}{-30 \times 10^{-6}} \times \frac{0.63}{-1.0} \times \frac{1.25 - 0.43 - 0.63/2}{1.25 - 0.4 - 1.0/2} = 3.5
\]

\[
(W/L)_p = 3.5 \times 1.5 = 5.25 \text{ for a } V_M \text{ of } 1.25V
\]
Simulated Inverter $V_M$

- $V_M$ is relatively insensitive to variations in device ratio
  - setting the ratio to 3, 2.5 and 2 gives $V_M$'s of 1.22V, 1.18V, and 1.13V

- Increasing the width of the PMOS moves $V_M$ towards $V_{DD}$
- Increasing the width of the NMOS moves $V_M$ toward GND

Note: x-axis is semilog

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Noise Margins Determining $V_{IH}$ and $V_{IL}$

By definition, $V_{IH}$ and $V_{IL}$ are where $dV_{out}/dV_{in} = -1$ (= gain)

- $V_{OH} = V_{DD}$
- $V_{OL} = GND$

- $NM_H = V_{DD} - V_{IH}$
- $NM_L = V_{IL} - GND$

Approximating:
- $V_{IH} = V_M - V_M /g$
- $V_{IL} = V_M + (V_{DD} - V_M) /g$

So high gain in the transition region is very desirable
CMOS Inverter VTC from Simulation

- **0.25um, (W/L)_p/(W/L)_n = 3.4**
- **(W/L)_n = 1.5 (min size)**
- **V_DD = 2.5V**
- **V_M ≈ 1.25V, g = -27.5**
- **V_IL = 1.2V, V_IH = 1.3V**
- **NM_L = NM_H = 1.2**
- (actual values are **V_IL = 1.03V, V_IH = 1.45V**
- **NM_L = 1.03V & NM_H = 1.05V**)
- **Output resistance**
  - low-output = 2.4kΩ
  - high-output = 3.3kΩ

Gain Determinates

- **Gain is a strong function of the slopes of the currents in the saturation region, for V_in = V_M**
- **g ≈ \frac{(1+r)}{(V_M-V_{Tn}-V_{DSATn}/2)(\lambda_n - \lambda_p)}**

Determined by technology parameters, especially channel length modulation (\lambda). Only designer influence through supply voltage and V_M (transistor sizing).
Impact of Process Variation on VTC Curve

process variations (mostly) cause a shift in the switching threshold

Scaling the Supply Voltage

Device threshold voltages are kept (virtually) constant