Review: CMOS Circuit Styles

- Static complementary CMOS - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - VOH and VOL are at VDD and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between VDD and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)

- Dynamic CMOS - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise
Review: Static Complementary CMOS

Pull-up network (PUN) and pull-down network (PDN)

PMOS transistors only
pull-up: make a connection from V_{DD} to F when \( F(\text{In}_1, \text{In}_2, \ldots, \text{In}_N) = 1 \)

NMOS transistors only
pull-down: make a connection from F to GND when \( F(\text{In}_1, \text{In}_2, \ldots, \text{In}_N) = 0 \)

PUN and PDN are dual logic networks

AOI221

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Pass Transistor Logic

• Primary inputs drive both gate and source/drain terminals
• NMOS switch closes when the gate input is high

\[ X = Y \text{ if } A \text{ and } B \]

\[ X = Y \text{ if } A \text{ or } B \]

• Remember –
NMOS transistors pass a strong 0 but a weak 1
PMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low

\[ X = Y \text{ if } A \text{ and } B = A + B \]

\[ X = Y \text{ if } A \text{ or } B = A \cdot B \]

- Remember – PMOS transistors pass a strong 1 but a weak 0

Pass Transistor (PT) Logic

- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)
VTC of PT AND Gate

Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

Differential PT Logic (CPL)

Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)
CPL Properties

- **Differential** so complementary data inputs and outputs are always available (so don’t need extra inverters)
- Still static, since the output defining nodes are always tied to $V_{DD}$ or GND through a low resistance path
- Design is **modular**; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like **adders**
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

CPL Full Adder

![CPL Full Adder Diagram]
**CPL Full Adder**

- **A**, **B**, and **Cin** are inputs.
- **Sum** and **Cout** are outputs.
- The circuit includes AND, OR, and NOT gates.

**NMOS Only PT Driving an Inverter**

- \( I_{in} = V_{DD} \)
- \( V_x = V_{DD} - V_{Tn} \)

- **Vx** does not pull up to **VDD**, but **VDD** – **Vtn**

- Threshold voltage drop causes static power consumption (\( M_2 \) may be weakly conducting forming a path from **VDD** to **GND**)

- Notice \( V_{Tn} \) increases of pass transistor due to body effect (**Vsb**)
 Voltage Swing of PT Driving an Inverter

Body effect – large $V_{SB}$ at $x$ - when pulling high ($B$ is tied to GND and $S$ charged up close to $V_{DD}$)

So the voltage drop is even worse

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{|2\phi_f| + V_x} - \sqrt{|2\phi_f|}))$$

Cascaded NMOS Only PTs

Pass transistor gates should never be cascaded as on the left

Logic on the right suffers from static power dissipation and reduced noise margins
Solution 1: Level Restorer

- Full swing on x (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when A is high
- For correct operation M_r must be sized correctly (ratioed)

Transient Level Restorer Circuit Response

- Restorer has speed and power impacts: increases the capacitance at x, slowing down the gate; increases $t_r$ (but decreases $t_f$)
**Solution 2: Multiple VT Transistors**

- Technology solution: Use (near) zero $V_T$ devices for the NMOS PTs to eliminate *most* of the threshold drop (body effect still in force preventing full swing to $V_{DD}$)

![Diagram showing multiple VT transistors with low $V_T$ transistors and sneak path](image)

- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if $V_{GS}$ is below $V_T$)

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**Solution 3: Transmission Gates (TGs)**

- Most widely used solution

![Diagram showing transmission gates](image)

- Full swing bidirectional switch controlled by the gate signal $C$, $A = B$ if $C = 1$
Solution 3: Transmission Gates (TGs)

- Most widely used solution

- Full swing bidirectional switch controlled by the gate signal C, A = B if C = 1

![Diagram of Transmission Gates]

Resistance of TG

![Graph showing resistance vs. output voltage]

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TG Multiplexer

\[ F = \overline{(In_1 \cdot S + In_2 \cdot \overline{S})} \]

Transmission Gate XOR

\[ A \oplus B \]
Transmission Gate XOR

\[ A \oplus B \]

\[ \text{weak 0 if } !A \]

\[ \text{weak 1 if } A \]

\[ \text{an inverter} \]

TG Full Adder

\[ C_{in} \]

\[ B \]

\[ A \]

\[ \text{Sum} \]

\[ C_{out} \]
Differential TG Logic (DPL)

\[ F = A \oplus B \]
\[ F = A \cap B \]

AND/NAND

XOR/XNOR