CPE/EE 427, CPE 527
VLSI Design I
Complementary CMOS Logic Gates

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Static CMOS Logic
CMOS Circuit Styles

- **Static complementary CMOS** - except during switching, output connected to either VDD or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - $V_OH$ and $V_OL$ are at VDD and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between VDD and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)

- **Dynamic CMOS** - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise

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**Static Complementary CMOS**

Pull-up network (PUN) and pull-down network (PDN)

PMOS transistors only
- pull-up: make a connection from $V_{DD}$ to $F$ when $F(I_{in1}, I_{in2}, \ldots I_{inN}) = 1$

NMOS transistors only
- pull-down: make a connection from $F$ to GND when $F(I_{in1}, I_{in2}, \ldots I_{inN}) = 0$

PUN and PDN are dual logic networks
Threshold Drops

PUN

\[ V_{DD} \rightarrow 0 \rightarrow V_{DD} - V_{Th} \]

PDN

\[ V_{DD} \rightarrow 0 \rightarrow |V_{tp}| \]
Construction of PDN

- NMOS devices in **series** implement a NAND function
  \[ A \cdot B \]
- NMOS devices in **parallel** implement a NOR function
  \[ A + B \]

Dual PUN and PDN

- PUN and PDN are dual networks
  - DeMorgan's theorems
    \[
    A + B = A \cdot B \\
    !(A + B) = !A \cdot !B \\
    A \cdot B = A + B \\
    !(A \cdot B) = !A + !B
    \]
  - A **parallel** connection of transistors in the PUN corresponds to a **series** connection of the PDN
  - Complementary gate is naturally **inverting** (NAND, NOR, AOI, OAI)
  - Number of transistors for an N-input logic gate is **2N**
CMOS NAND

A • B

F = NAND(A, B)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

CMOS NAND

F = NAND(A, B)

9/18/2006  VLSI Design I;  A. Milenkovic
CMOS NOR

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
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<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

F = \overline{A + B}

CMOS NOR

F = \overline{A \cdot B}

\begin{align*}
A = 0 & \quad B = 0 \\
F &= 1 \\
GND &
\end{align*}

\begin{align*}
A = 0 & \quad B = 1 \\
F &= 0 \\
GND &
\end{align*}

\begin{align*}
A = 1 & \quad B = 0 \\
F &= 1 \\
GND &
\end{align*}

\begin{align*}
A = 1 & \quad B = 1 \\
F &= 0 \\
GND &
\end{align*}
Complex CMOS Gate

OUT = !(D + A • (B + C))

Complex CMOS Gate

OUT = !(D + A • (B + C))
XNOR/XOR Implementation

<table>
<thead>
<tr>
<th>XNOR</th>
<th>XOR</th>
</tr>
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<tbody>
<tr>
<td><img src="image1" alt="XNOR Circuit" /></td>
<td><img src="image2" alt="XOR Circuit" /></td>
</tr>
</tbody>
</table>

- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?

Combinational Logic Cells

- CMOS logic cells
  - AND-OR-INVERT (AOI)
  - OR-AND-INVERT (OAI)
- Example: AOI221
  \[ Z = (A\cdot B + C\cdot D + E)' \]
  \[ Z = AOI221(A, B, C, D, E) \]
  Exercise: Construct this logic cell?
- Example: OAI321
  \[ Z = [(A+B+C)\cdot (D+E)\cdot F]' \]
  \[ Z = OAI321(A, B, C, D, E, F) \]
  Exercise: Construct this logic cell?
What logic function is this?
OAI21 Logic Graph

\[ X = !(C \cdot (A + B)) \]

Two Stick Layouts of \(! (C \cdot (A + B))\)

uninterrupted diffusion strip
Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)
Some functions have no consistent Euler path like $x = !(a + bc + de)$ (but $x = !(bc + a + de)$ does!)
Combinational Logic Cells (cont’d)

- The AOI family of cells with 3 index numbers or less
  - \( X = \{\text{AOI, OAI, AO, OA}\}; a, b, c = \{2, 3\} \)

<table>
<thead>
<tr>
<th>Cell Type</th>
<th>Cells</th>
<th>Number of Unique Cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xa1</td>
<td>X21, X31</td>
<td>2</td>
</tr>
<tr>
<td>Xa11</td>
<td>X211, X311</td>
<td>2</td>
</tr>
<tr>
<td>Xab</td>
<td>X22, X33, X32</td>
<td>3</td>
</tr>
<tr>
<td>Xab1</td>
<td>X221, X321, X331</td>
<td>3</td>
</tr>
<tr>
<td>Xabc</td>
<td>X222, X333, X332, X322</td>
<td>4</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>14</strong></td>
</tr>
</tbody>
</table>

VTC is Data-Dependent

- The threshold voltage of \( M_2 \) is higher than \( M_1 \) due to the body effect (\( \gamma \))
  \[
  V_{Tn1} = V_{Tn0} \\
  V_{Tn2} = V_{Tn0} + \gamma (\sqrt{2\phi_F + V_{int}} - \sqrt{2\phi_F})
  \]
  since \( V_{SB} \) of \( M_2 \) is not zero (when \( V_B = 0 \)) due to the presence of \( C_{int} \)
Static CMOS Full Adder Circuit

C\text{out} = C_{in} \& (A \mid B) \mid (A \& B) \quad \text{Sum} = !C_{out} \& (A \mid B \mid C_{in}) \mid (A \& B \& C_{in})

!C\text{out} = !C_{in} \& (!A \mid !B) \mid (!A \& !B)

Sum = !C_{out} \& (A \mid !B \mid !C_{in}) \mid (!A \& !B \& !C_{in})