CPE/EE 427, CPE 527
VLSI Design I
MOS Transistor Theory

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Outline

• Introduction
• MOS Capacitor
• nMOS I-V Characteristics
• pMOS I-V Characteristics
• Gate and Diffusion Capacitance
• Non-Ideal IV Effects
Introduction

• So far, we have treated transistors as ideal switches
• An ON transistor passes a finite amount of current
  – Depends on terminal voltages
  – Derive current-voltage (I-V) relationships
• Transistor gate, source, drain all have capacitance
  – \( I = C \left( \Delta V / \Delta t \right) \rightarrow \Delta t = (C/I) \Delta V \)
  – Capacitance and current determine speed
• Also explore what a “degraded level” really means

MOS Capacitor

• Gate and body form MOS capacitor
• Operating modes
  – Accumulation
  – Depletion
  – Inversion
Terminal Voltages

- Mode of operation depends on $V_{g}$, $V_{d}$, $V_{s}$
  - $V_{gs} = V_{g} - V_{s}$
  - $V_{gd} = V_{g} - V_{d}$
  - $V_{ds} = V_{d} - V_{s} = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - Cutoff
  - Linear
  - Saturation

nMOS Cutoff

- No channel
- $I_{ds} = 0$
nMOS Linear

- Channel forms
- Current flows from d to s
  - e⁻ from s to d
- $I_{ds}$ increases with $V_{ds}$
- Similar to linear resistor

\[ V_{gs} > V_t \]
\[ V_{gs} > V_{gd} > V_t \]
\[ V_{ds} = 0 \]
\[ 0 < V_{gs} < V_{gs}-V_t \]

\[ I_{ds} \]

nMOS Saturation

- Channel pinches off
- $I_{ds}$ independent of $V_{ds}$
- We say current saturates
- Similar to current source

\[ V_{gs} > V_t \]
\[ V_{gs} < V_t \]
\[ V_{ds} = V_{gs}-V_t \]
\[ 0 < V_{gs} < V_{gs}-V_t \]
I-V Characteristics

- In Linear region, $I_{ds}$ depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel

\[ Q_{\text{channel}} = \]
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C = C_g = \varepsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}} WL$
- $V = V_s - V_g - V_d$

\[ C_{\text{ox}} = \varepsilon_{\text{ox}} / t_{\text{ox}} \]
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- $Q_{\text{channel}} = CV$
- $C = C_g = \varepsilon_{\text{ox}} WL/t_{\text{ox}} = C_{\text{ox}} WL$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$

Carrier velocity

- Charge is carried by $e^-$
- Carrier velocity $v$ proportional to lateral E-field between source and drain
- $v =$

[Diagrams of MOS structure and carrier velocity]
Carrier velocity

• Charge is carried by e-
• Carrier velocity \( v \) proportional to lateral E-field between source and drain
  • \( v = \mu E \) \( \mu \) called mobility
  • \( E = \frac{V_{ds}}{L} \)
  • Time for carrier to cross channel:
    – \( t = \)
Carrier velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
- $v = \mu E$ $\mu$ called mobility
- $E = V_{ds}/L$
- Time for carrier to cross channel:
  - $t = L / v$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{\text{channel}}$ is in the channel
  - How much time $t$ each carrier takes to cross

$$I_{ds} =$$
Now we know
- How much charge $Q_{\text{channel}}$ is in the channel
- How much time $t$ each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds}$$

$$= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds}$$

$\beta = \mu C_{ox} \frac{W}{L}$
nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

\[ I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{dsat} \]
nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{sat}$$

$$I_{ds} = \frac{\beta}{2} \left( V_{gs} - V_t \right)^2$$

nMOS I-V Summary

- **Shockley 1st order transistor models**

$$I_{ds} = \begin{cases} 
0 & V_{gs} < V_t \text{ cutoff} \\
\beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \text{ linear} \\
\frac{\beta}{2} \left( V_{gs} - V_t \right)^2 & V_{ds} > V_{dsat} \text{ saturation} 
\end{cases}$$
Example

- For a 0.6 µm process
  - From AMI Semiconductor
  - $t_{ox} = 100$ Å
  - $\mu = 350$ cm$^2$/V*s
  - $V_t = 0.7$ V
- Plot $I_{ds}$ vs. $V_{ds}$
  - $V_{gs} = 0, 1, 2, 3, 4, 5$
  - Use $W/L = 4/2 \lambda$

\[
\beta = \mu C_m \frac{W}{L} = (350) \left( \frac{3.9 \times 8.85 \times 10^{-14}}{100 \times 10^{-6}} \right) \left( \frac{W}{L} \right) = 120 \frac{W}{L} \mu A/V^2
\]

pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility $\mu_p$ is determined by holes
  - Typically 2-3x lower than that of electrons $\mu_n$
  - 120 cm$^2$/V*s in AMI 0.6 µm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$
  - *** plot I-V here
Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance (simple model)

- Approximate channel as connected to source
- \( C_{gs} = \varepsilon_{ox} WL/t_{ox} = C_{ox} WL = C_{permicron} W \)
- \( C_{permicron} \) is typically about 2 fF/\( \mu \)m
Diffusion Capacitance (simple model)

- $C_{sb}$, $C_{db}$
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to $C_g$ for contacted diff
  - $\frac{1}{2} C_g$ for uncontacted
  - Varies with process

MOS Structure Capacitances

- Overlap capacitance (linear)
- $C_{GSO} = C_{GDO} = C_{ox} x_d W = C_o W$
MOS Channel Capacitances

• The gate-to-channel capacitance depends upon the operating region and the terminal voltages

\[ C_{GS} = C_{GCS} + C_{GSO} \]
\[ C_{GD} = C_{GCD} + C_{GDO} \]

\[ C_{GB} = C_{GCB} \]

Average Distribution of Channel Capacitance

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>( C_{GCB} )</th>
<th>( C_{GCS} )</th>
<th>( C_{GCD} )</th>
<th>( C_{GC} )</th>
<th>( C_{G} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>( C_{ox}WL )</td>
<td>0</td>
<td>0</td>
<td>( C_{ox}WL )</td>
<td>( C_{ox}WL + 2C_{ox}W )</td>
</tr>
<tr>
<td>Resistive</td>
<td>0</td>
<td>( C_{ox}WL/2 )</td>
<td>( C_{ox}WL/2 )</td>
<td>( C_{ox}WL )</td>
<td>( C_{ox}WL + 2C_{ox}W )</td>
</tr>
<tr>
<td>Saturation</td>
<td>0</td>
<td>((2/3)C_{ox}WL)</td>
<td>0</td>
<td>((2/3)C_{ox}WL)</td>
<td>((2/3)C_{ox}WL + 2C_{ox}W)</td>
</tr>
</tbody>
</table>

• Channel capacitance components are nonlinear and vary with operating voltage
• Most important regions are cutoff and saturation since that is where the device spends most of its time
**MOS Diffusion Capacitances**

- The junction (or diffusion) capacitance is from the reverse-biased source-body and drain-body pn-junctions.

\[ C_{SB} = C_{Sdiff} \quad \text{and} \quad C_{DB} = C_{Ddiff} \]

**Source Junction View**

\[ C_{diff} = C_{bp} + C_{sw} = C_j \text{AREA} + C_{jsw} \text{PERIMETER} \]

\[ = C_j L_S W + C_{jsw} (2L_S + W) \]
Recap: The Diode

Cross-section of $p-n$ junction in an IC process

One-dimensional representation
diode symbol

*Mostly occurring as parasitic element in Digital ICs*

Recap: Depletion Region

(a) Current flow.
(b) Charge density.
(c) Electric field.
(d) Electrostatic potential.
Recap: Diode Current

The ideal diode equation (for both forward and reverse-bias conditions) is

\[ I_D = I_S (e^{V_D/\phi_T} - 1) \]

where \( V_D \) is the voltage applied to the junction

- a forward-bias lowers the potential barrier allowing carriers to flow across the diode junction
- a reverse-bias raises the potential barrier and the diode becomes nonconducting

\( \phi_T = kT/q = 26mV \) at 300K

\( I_S \) is the saturation current of the diode

Recap: Ideal Diode Equation

• The ideal diode equation (for both forward and reverse-bias conditions) is

\[ I_D = I_S (e^{V_D/\phi_T} - 1) \]

where \( V_D \) is the voltage applied to the junction

- a forward-bias lowers the potential barrier allowing carriers to flow across the diode junction
- a reverse-bias raises the potential barrier and the diode becomes nonconducting

\( \phi_T = kT/q = 26mV \) at 300K

\( I_S \) is the saturation current of the diode
MOS Diffusion Capacitances

\[ C_{\text{diff}} = C_{bp} + C_{sw} = C_{jbp} \text{ AREA} + C_{jsw} \text{ PERIMETER} \]
\[ = C_{jbp} L_S W + C_{jsw} (2L_S + W) \]

Source parasitic:
\[ C_{jbs} = C_J (1+V_{sb}/\psi_0)^{-Mj} \]
- \( C_J \) – junction capacitance at zero bias
- \( Mj \) – junction grading coefficient (0.5 – 0.33)
- \( \psi_0 \) – built-in potential \( \psi_0 = \nu_T \ln(N_A N_D/\eta_i^2) \)

\[ C_{jbsw} = C_{JSW} (1+V_{sb}/\psi_0)^{-Mjsw} \]
- \( C_{JSW} \) – junction capacitance at zero bias
- \( Mjsw \) – junction grading coefficient (0.5 – 0.33)

MOS Capacitance Model

\[ C_{GS} = C_{GCS} + C_{GSO} \]
\[ C_{GD} = C_{GCD} + C_{GDO} \]
\[ C_{SB} = C_{Sdiff} \]
\[ C_{DB} = C_{Ddiff} \]
\[ C_{GB} = C_{GCB} \]
### Transistor Capacitance Values for 0.25μ

Example: For an NMOS with \(L = 0.24\ \mu\text{m}, W = 0.36\ \mu\text{m},\) \(L_D = L_S = 0.625\ \mu\text{m}\)

\[
C_{\text{GSO}} = C_{\text{GDO}} = C_{\text{ox}} \times d = C_o \times W = \]
\[
C_{\text{GC}} = C_{\text{ox}} \times WL =
\]
so \(C_{\text{gate\_cap}} = C_{\text{ox}} \times WL + 2C_o \times W =
\]
\[
C_{\text{bp}} = C_j \times L_S \times W =
\]
\[
C_{\text{sw}} = C_{j\text{sw}} \times (2L_S + W) =
\]
so \(C_{\text{diffusion\_cap}} = \)

<table>
<thead>
<tr>
<th></th>
<th>(C_{\text{ox}} ) (fF/(\mu\text{m}))</th>
<th>(C_o ) (fF/(\mu\text{m}))</th>
<th>(C_j ) (fF/(\mu\text{m}))</th>
<th>(m_j )</th>
<th>(\phi_b ) (V)</th>
<th>(C_{j\text{sw}} ) (fF/(\mu\text{m}))</th>
<th>(m_{j\text{sw}} )</th>
<th>(\phi_{b\text{sw}} ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>6</td>
<td>0.31</td>
<td>2</td>
<td>0.5</td>
<td>0.9</td>
<td>0.28</td>
<td>0.44</td>
<td>0.9</td>
</tr>
<tr>
<td>PMOS</td>
<td>6</td>
<td>0.27</td>
<td>1.9</td>
<td>0.48</td>
<td>0.9</td>
<td>0.22</td>
<td>0.32</td>
<td>0.9</td>
</tr>
</tbody>
</table>
Non-Ideal I-V Effects

- $I_{ds}(\text{sat})$ increases less than quadratically with increasing $V_{gs}$
  - Velocity saturation & mobility degradation

- $I_{ds}(\text{sat})$ increases slightly with $V_{ds}$
  - Channel length modulation

- $V_T$ is influenced by the $V_{sb}$
  - Body effect

- There is current flow in nominally OFF transistors
  - Subthreshold conduction (junction leakage, tunnel)

\[
I_{ds} = \begin{cases} 
0 & V_{gs} < V_T \quad \text{cutoff} \\
\beta \left(V_{gs} - V_T + \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{sat} \quad \text{linear} \\
\frac{\beta}{2} (V_{gs} - V_T)^2 & V_{ds} > V_{sat} \quad \text{saturation}
\end{cases}
\]

Current Determinates

- For a fixed $V_{DS}$ and $V_{GS} (> V_T)$, $I_{DS}$ is a function of
  - the distance between the source and drain – $L$
  - the channel width – $W$
  - the threshold voltage – $V_T$
  - the thickness of the SiO$_2$ – $t_{ox}$
  - the dielectric of the gate insulator (SiO$_2$) – $\varepsilon_{ox}$
  - the carrier mobility
    - for nfets: $\mu_n = 500 \text{ cm}^2/\text{V-sec}$
    - for pfets: $\mu_p = 180 \text{ cm}^2/\text{V-sec}$
Long Channel I-V Plot (NMOS)

- $I_D$ vs $V_{DS}$ for different $V_{GS}$
- Linear and Saturation regions
- Quadratic dependence

Short Channel Effects

- Behavior of short channel device mainly due to:
  - $\nu_{sat} = 10^5$
- Velocity saturation – the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

- For an NMOS device with $L = 0.25\mu m$, only a couple of volts difference between D and S are needed to reach velocity saturation
Voltage-Current Relation: Velocity Saturation

For short channel devices

- Linear: When $V_{DS} \leq V_{GS} - V_T$
  \[ I_D = \kappa(V_{DS}) k'_n \frac{W}{L} [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \]
  where
  \[ \kappa(V) = \frac{1}{1 + (V/\xi_cL)} \]
  is a measure of the degree of velocity saturation

- Saturation: When $V_{DS} = V_{DSAT} \geq V_{GS} - V_T$
  \[ I_{DSat} = \kappa(V_{DSAT}) k'_n \frac{W}{L} [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2] \]

Velocity Saturation Effects

For short channel devices and large enough $V_{GS} - V_T$

- $V_{DSAT} < V_{GS} - V_T$ so the device enters saturation before $V_{DS}$ reaches $V_{GS} - V_T$ and operates more often in saturation

- $I_{DSAT}$ has a linear dependence wrt $V_{GS}$ so a reduced amount of current is delivered for a given control voltage
Short Channel I-V Plot (NMOS)

NMOS transistor, 0.25\,\mu\text{m}, L_d = 0.25\,\mu\text{m}, W/L = 1.5, V_{DD} = 2.5\,\text{V}, V_T = 0.4\,\text{V}

MOS I_D-V_{GS} Characteristics

• Linear (short-channel) versus quadratic (long-channel) dependence of $I_D$ on $V_{GS}$ in saturation
• Velocity-saturation causes the short-channel device to saturate at substantially smaller values of $V_{DS}$ resulting in a substantial drop in current drive

(for $V_{DS} = 2.5\,\text{V}, W/L = 1.5$)
Short Channel I-V Plot (PMOS)

- All polarities of all voltages and currents are reversed

\[ V_{DS} (V) \]

\[ I_D (A) \]

- \( V_{GS} = -1.0V \)
- \( V_{GS} = -1.5V \)
- \( V_{GS} = -2.0V \)
- \( V_{GS} = -2.5V \)

PMOS transistor, 0.25um, \( L_d = 0.25um \), \( W/L = 1.5 \), \( V_{DD} = 2.5V \), \( V_T = -0.4V \)

Transistor in Saturation Mode

Assuming \( V_{GS} > V_T \)

The current remains constant (saturates).
Voltage-Current Relation: Saturation Mode

For long channel devices
- When $V_{DS} \geq V_{GS} - V_T$

$$I_D' = \frac{k'n}{2} \frac{W}{L} \left[(V_{GS} - V_T)^2\right]$$

since the voltage difference over the induced channel (from the pinch-off point to the source) remains fixed at $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied $V_{DS}$, so

$$I_D = I_D' \left(1 + \lambda V_{DS}\right)$$

where $\lambda$ is the channel-length modulation (varies with the inverse of the channel length)

Threshold Voltage Concept

The value of $V_{GS}$ where strong inversion occurs is called the threshold voltage, $V_T$
The Threshold Voltage

\[ V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \]

where

- \( V_{T0} \) is the threshold voltage at \( V_{SB} = 0 \) and is mostly a function of the manufacturing process
  - Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.
- \( V_{SB} \) is the source-bulk voltage
- \( \phi_F = -\phi_T \ln(N_A/n_i) \) is the Fermi potential \((\phi_T = kT/q = 26\text{mV at }300\text{K is the thermal voltage}; N_A \text{ is the acceptor ion concentration}; n_i \approx 1.5\times10^{10} \text{cm}^{-3} \text{ at }300\text{K is the intrinsic carrier concentration in pure silicon})
- \( \gamma = \sqrt{(2q\varepsilon_{si} N_A)/C_{ox}} \) is the body-effect coefficient (impact of changes in \( V_{SB} \) \((\varepsilon_{si}=1.053\times10^{-10}\text{F/m is the permittivity of silicon}; C_{ox} = \varepsilon_{ox}/t_{ox} \text{ is the gate oxide capacitance with } \varepsilon_{ox}=3.5\times10^{-11}\text{F/m})

The Body Effect

- \( V_{SB} \) is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes \( V_T \) to increase from 0.45V to 0.85V
Other (Submicon) MOS Transistor Concerns

- Velocity saturation
- Subthreshold conduction
  - Transistor is already partially conducting for voltages below VT
- Threshold variations
  - In long-channel devices, the threshold is a function of the length (for low VDS)
  - In short-channel devices, there is a drain-induced threshold barrier lowering at the upper end of the VDS range (for low L)
- Parasitic resistances
  - resistances associated with the source and drain contacts
- Latch-up

Subthreshold Conductance

- Transition from ON to OFF is gradual (decays exponentially)
- Current roll-off (slope factor) is also affected by increase in temperature

\[ S = n \left(\frac{kT}{q}\right) \ln(10) \]
(typical values 60 to 100 mV/decade)

- Has repercussions in dynamic circuits and for power consumption

\[ I_D \sim I_S e^{\left(\frac{qV_{GS}}{nkT}\right)} \quad \text{where} \quad n \geq 1 \]
Subthreshold $I_D$ vs $V_{GS}$

Subthreshold MOS Characteristics: 55nm, 0.3V process

$$I_D = I_S \ e^{\frac{q(V_{GS}-V_{TH})}{nkT}} \ (1 - e^{-\frac{qV_{DS}}{nkT}})(1 + \lambda V_{DS})$$

$V_{DS}$ from 0 to 0.5V

Subthreshold $I_D$ vs $V_{DS}$

Subthreshold MOS Characteristics: 55nm, 0.3V process

$$I_D = I_S \ e^{\frac{qV_{GS}}{nkT}} \ (1 - e^{-\frac{qV_{DS}}{nkT}})(1 + \lambda V_{DS})$$

$V_{GS}$ from 0 to 0.3V
Threshold Variations

Threshold as a function of the length (for low \(V_{DS}\))

Drain-induced barrier lowering (for low \(L\))

Voltage-Current Relation: Linear Mode

For long-channel devices (\(L > 0.25\) micron)

- When \(V_{DS} \leq V_{GS} - V_{T}\)
  \[
  I_D = k'_n \frac{W}{L} \left[ (V_{GS} - V_{T})V_{DS} - V_{DS}^2/2 \right]
  \]
  where
  \[
  k'_n = \mu_n C_{ox} = \frac{\mu_n e_{ox}}{t_{ox}} = \text{is the process transconductance parameter (} \mu_n \text{ is the carrier mobility (m}^2/\text{Vsec))}
  \]
  \[
  k_n = k'_n \frac{W}{L} = \text{is the gain factor of the device}
  \]
- For small \(V_{DS}\), there is a linear dependence between \(V_{DS}\) and \(I_D\), hence the name resistive or linear region
The MOS Current-Source Model

\[ I_D = 0 \text{ for } V_{GS} - V_T \leq 0 \]
\[ I_D = k' \frac{W}{L} [(V_{GS} - V_T)V_{min} - V_{min}^2/2](1 + \lambda V_{DS}) \]
for \( V_{GS} - V_T \geq 0 \)

\[ V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT}) \]
and \( V_{GT} = V_{GS} - V_T \)

\( \lambda (V^{-1}) \)
\( (V_{0.5}) \)
\( \gamma (V^{0.5}) \)
\( V_{DSAT} (V) \)
\( V_{T0} (V) \)
\( k'(A/V^2) \)

<table>
<thead>
<tr>
<th></th>
<th>V_{T0} (V)</th>
<th>\gamma (V^{0.5})</th>
<th>V_{DSAT} (V)</th>
<th>k' (A/V^2)</th>
<th>\lambda (V^{-1})</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.43</td>
<td>0.4</td>
<td>0.63</td>
<td>115 x 10^{6}</td>
<td>0.06</td>
</tr>
<tr>
<td>PMOS</td>
<td>-0.4</td>
<td>-0.4</td>
<td>-1</td>
<td>-30 x 10^{6}</td>
<td>-0.1</td>
</tr>
</tbody>
</table>

Determined by the voltages at the four terminals and a set of five device parameters.

The Transistor Modeled as a Switch

\( R_{on} \) (for \( W/L = 1 \))

<table>
<thead>
<tr>
<th>V_{DD} (V)</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS (kΩ)</td>
<td>35</td>
<td>19</td>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>PMOS (kΩ)</td>
<td>115</td>
<td>55</td>
<td>38</td>
<td>31</td>
</tr>
</tbody>
</table>

Modeled as a switch with infinite off resistance and a finite on resistance, \( R_{on} \)

- Resistance inversely proportional to \( W/L \) (doubling \( W \) halves \( R_{on} \))
- For \( V_{DD} \gg V_T + V_{DSAT}/2 \), \( R_{on} \) independent of \( V_{DD} \)
- Once \( V_{DD} \) approaches \( V_T \), \( R_{on} \) increases dramatically

\( R_{eq} \) (\( \Omega \) for \( V_{GS} = V_{DD}, V_{DS} = V_{DD}/2 \))

For larger devices divide \( R_{eq} \) by \( W/L \)
Next Time: The CMOS Inverter

\[ \text{Next Time: The CMOS Inverter} \]