

Quiz – EXAMPLE QUESTIONS

1. Simplify the following equation using only algebraic manipulations. Show all the steps.

$$F = ABC + ACD + ABD + ABC\bar{C} + \bar{A}CD + AB\bar{D}$$

2. For the following truth table generate SOP (sum of products) equation for F

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

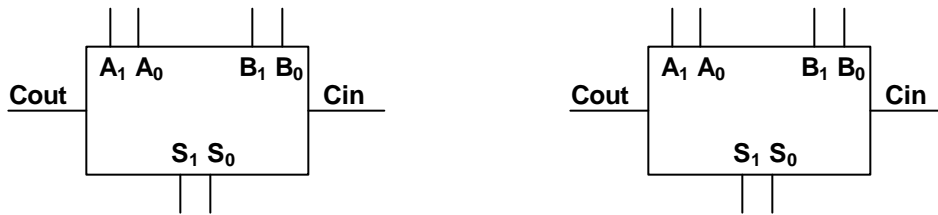
3. Implement equation $F = A + BC$ using NAND gates only. Use gate equivalency rules and show all the steps.

4. Minimize function F (given by the truth table) using K-Maps

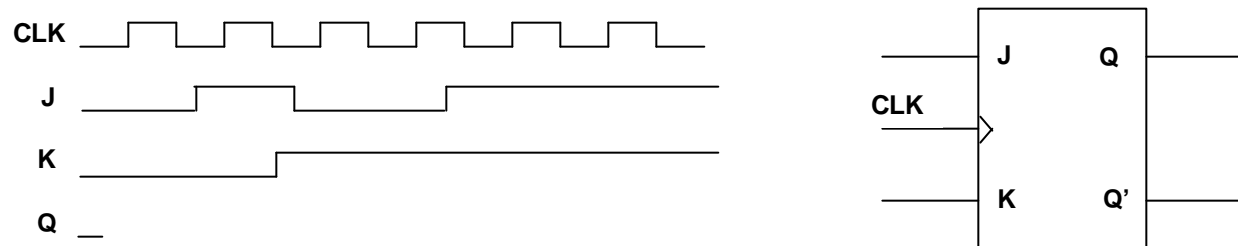
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	X
1	0	0	1	X
1	0	1	0	X
1	0	1	1	X
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

5. Implement the function $F = ABC\bar{C} + \bar{A}BC$ using only one 4-to-1 multiplexor (hint: produce truth table first)

6. Construct a 4-bit adder using two 2-bit full adders. If the numbers $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$ are to be added, show where each of these 8 bits will be connected (X_3 to X_0 and Y_3 to Y_0). Show where the four bits of the result ($\Sigma_3\Sigma_2\Sigma_1\Sigma_0$) will come from, as well as the final carry out.



7. Finish the timing diagram for the standard JK FF and the signals CLK, J, and K as given in the timing diagram.



8. Design a divide-by-5 counter using a standard 3-bit ripple counter and any other standard gates you might need (AND, NAND, OR, ...). [CLEAR': Asynchronous clear, CLK – clock, Q_a is the least significant bit.]

