

Digital Logic Design Lab (EE 201-05)

1 Credit hr. (Fall 2002), Wednesday 1 – 4 pm, EB 227

<i>Instructor</i>	DEJAN RASKOVIC
<i>Email</i>	raskovd@ece.uah.edu (the best and the fastest way to contact me)
<i>Course Web page</i>	http://www.ece.uah.edu/~raskovd/EE201
<i>Office Hours</i>	Thursday, 2 – 3 pm
<i>Office</i>	EB 242B
<i>Text Book</i>	Digital Logic Design–Tutorials and Laboratory Exercises
<i>Authors</i>	John F. Passifume and Michael Douglas
<i>Additional material</i>	EE 201 Supplement Package

General Course Objectives

1. To give you the ability to *design, build, analyze, and test* simple digital circuits that meet given sets of specifications. These skills will provide the foundation for design-oriented courses involving digital signal processing systems, VLSI design, computer design and microprocessor-based design.
2. To provide experience in use of computer-aided design tools (ALTERA MAX+PLUS II Logic Design) for digital circuit design and analysis.

Examinations and Grading. The distribution of grades is also mentioned in the supplement and explained during the first class.

PreLabs	25%
In-Lab Work	30%
Quiz	5%
Lab Reports	20%
Final Project	20%

Lab Reports. These reports are due beginning of the next lab (in other words, you will always have one week to prepare your report). Report has to follow a template given in the EE 201 Supplement Package. **Late work will be penalized with a 10% reduction in grade per day. Reports turned in later than one week will not be accepted. Also, late reports will not be accepted during the last week of classes.**

PreLabs. PreLab assignments usually consist of three to four problems to be solved and designs to be prepared for the next week's lab. **PreLabs have to be turned in each Monday, before 1:00 pm.** Late work will be graded and returned if you submit it before the lab starts, but will be penalized with a 50% reduction in grade.

Quiz. One quiz will be given during regular lab hours, close to the end of this course. Exact date and material to be covered will be announced one week in advance.

Absence policy. Student must complete all four phases for each lab (pre-lab assignment, simulation, experiment, and report) and complete the final project to receive full credit. Therefore, there will be a certain reduction of a letter grade towards your final grade for each lab missed without a good reason.

Final Project. There is a final project that every student has to complete. Project will include simulation and design of a fairly complex digital system that includes most of the components used during the course.

Additional info

Students are required to send an email message containing first and last name as it appears on student's record, preferred name, and a valid email address to the instructor:

raskovd@ece.uah.edu

You can ask any question related to this course using this email address, and I will try to answer your questions as soon as possible. You are also very welcome to come to my office during office hours (see above) to ask questions.