1. (12 points) (3 points) Write an entity for a 4-bit comparator which has 2 4-bit inputs and outputs a '1' if all of the bits match and a '0' otherwise. (9 points) Use concurrent signal assignments to model this comparator.

```vhdl
entity comparator is
  port ( a : bit vector (3 downto 0); b : bit vector (3 downto 0); check : out bit );
end comparator;

architecture concurrent of comparator is
begin
  check <= not (temp0 or temp1 or temp2 or temp3);
  temp0 <= a(0) xor b(0);
  temp1 <= a(1) xor b(1);
  temp2 <= a(2) xor b(2);
  temp3 <= a(3) xor b(3);
end concurrent;
```

2. (1 point) A **package** is a collection of commonly used data types and subprograms used in a design.

3. (1 point) A variable assignment is identified by the symbol **<=**.

4. (8 points) For the following declarations, are the given assignments valid?

```vhdl
SIGNAL count : BIT_VECTOR (1 TO 9);
ALIAS sign : BIT IS count (1);
ALIAS msd : BIT_VECTOR (1 TO 4) IS count (2 TO 5);
ALIAS lsd : BIT_VECTOR (1 TO 4) IS count (6 TO 9);
```

```vhdl
sign <= "10";
msd <= "1001";
count <= "110010000";
lsd <= sign;
```
5. (15 points) Design a resetting Moore machine that detects the number 9, encoded in binary, 1001, and excess-3 1100. Sample input (X) and output (Z) sequences are given below.

\[ \begin{align*}
X &= 100110001100... \\
Z &= 000100000001...
\end{align*} \]

entity detect9 is
\[
\text{port (sig-in : in bit,}
\text{CLK : in bit,}
\text{reset : in bit);}
\]
end entity detect9;

architecture state-machine of detect9 is
type state_type is (Init, one, one-zero, one-two-zero-one);
signal state : state_type;
beginn
process (CLK)
begin
if (CLK = '1' and (reset = '1')) then
if (reset = '1') then
state <= Init;
end if;
else
end if;
end process;
end

H. (1 point) An entity X, when used in another entity Y, becomes a _component_ for the entity Y.

7. (2 points) For the following function call, which function will be called?

\[
\text{VARIABLE a, b : INTEGER;}
\text{b := decrement (a);}
\]

(a) FUNCTION decrement (x : INTEGER) RETURN INTEGER;
(b) FUNCTION decrement (x : REAL) RETURN REAL

end state-machine;
8. (10 points) Draw the state diagram for the following state machine. Is it Moore or Mealy?

```vhdl
entity STATE_MACHINE is
  port (SIG_IN : in BIT; CLK : in BIT;
        SIG_OUT : out BIT);
end STATE_MACHINE;

architecture STATE_MACHINE of STATE_MACHINE is
  
  type STATE_TYPE is (A, B, C);
  signal STATE : STATE_TYPE := A;
begin
  process (CLK)
  begin
    if (CLK = '1' and CLK'EVENT) then
      if (STATE = A) then
        if (SIG_IN = '1') then
          STATE <= B;
        end if;
      elsif (STATE = B) then
        if (SIG_IN = '1') then
          STATE <= C;
        end if;
      elsif (STATE = C) then
        STATE <= A;
      end if;
    end if;
  end process

  with STATE select
  begin
    SIG_OUT <= '1' when A,
               '0' when B,
               '1' when C;
  end STATE_MACHINE;
end
```

9. (5 points) Write a process statement that will have the same effect as the following concurrent signal assignment statement.

```vhdl
with 2 select
A <= transport X and Y when 0, X or Y when 1, not X when others;
process (Z, X, Y)
begin
  if (Z = '0') then
    A <= transport (X and Y);
  elsif (Z = '1') then
    A <= transport (X or Y);
  else
    A <= transport (not X);
  end if;
end process;
```
10. (15 points) (a) (5 points) Create entity declarations and architecture body pairs for:
   a. and2
   c. not

   (b) (5 points) Create a package with component declarations for the entities defined previously.

   (c) (5 points) Implement the equation \( f = ab' \) using the components in the package created.

11. (10 points) Specify type declarations for the following data types.

   a. (3 points) A MONTH_OF_YEAR enumeration data type.
   
   ```
   type month_of_year is (Jan, Feb, Mar, Apr, May, June, Jul, Aug, Sept, Oct, Nov, Dec);
   ```

   b. (2 points) A data type DAY_OF_YEAR that can have integer values in the range from 1 to 366:
   
   ```
   type day_of_year is integer range 1 to 366;
   ```

   c. (2 points) An ascending range data type INC_8 with integer values from 0 to 7.
   
   ```
   type inc_8 is integer range 0 to 7;
   ```

   d. (3 points) A 1-bit descending-index register composite data type, REGISTER_8_BIT_ASCENDING, with index values from the type INC_8 declared above, and component values of type BIT.
   
   ```
   type register_8_bit_ascending is array (inc_8) of bit;
   ```
12. (4 points) Write declarations for the following constants, variables, or signals. Refer to the data types defined in Problem 11.
   
   a. (1 point) A constant MID_YEAR that has value JUNE of type MONTH_OF_YEAR.
   
   ```vhdl
   constant mid_year : month_of_year := june;
   ```
   
   b. (1 point) A signal HOLIDAY of type DAY_OF_YEAR.
   
   ```vhdl
   signal holiday : day_of_year;
   ```
   
   c. (2 points) A variable NUMBER which is initialized to the 8-bit representation for (-1) in two's complement notation of type REGISTER_8_BIT_ASCENDING.
   
   ```vhdl
   variable number : register_8_bit_ascending := "11111111";
   ```
   
13. (15 points) Write a VHDL procedure that counts the number of 1's, 0's and Z's in a std_logic_vector. The procedure must be general, i.e., it must accept an input parameter of arbitrary length.
   
   ```vhdl
   procedure one_zero_z (a : in std_logic_vector; one, zero, z : out integer) is
   variable temp_one, temp_zero, temp_z : integer;
   begin
   temp_one := 0;
   temp_zero := 0;
   temp_z := 0;
   for i in a'range loop
   if (a(i) = '0') then
   temp_zero := temp_zero + 1;
   elsif (a(i) = '1') then
   temp_one := temp_one + 1;
   elsif (a(i) = 'Z') then
   temp_z := temp_z + 1;
   end if;
   end loop;
   ```
   
14. (1 point) All statements inside of a subprogram are ________.
   
15. (1 point) A process is executed whenever ________ signals in the sensitiv list ________ an event.
   
   ```vhdl
   process (signal) begin
   if signal = not a then
   end if;
   ```