
Web Page: [http://www.ece.uah.edu/courses/cpe526](http://www.ece.uah.edu/courses/cpe526)

Instructor: Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573, email: gaede@ece.uah.edu

Office Hours: M 2:00 PM – 3:00 PM, TR 11:00 AM - 12:00 PM, or by appointment

Grading:  
<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework</td>
<td>20%</td>
</tr>
<tr>
<td>Project</td>
<td>25%</td>
</tr>
<tr>
<td>Midterm</td>
<td>25%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>30%</td>
</tr>
</tbody>
</table>

Homework: NO late homework will be accepted without extenuating circumstances. Contact me as soon as a problem occurs.

Important Dates:  
- January 11 – Last day to add a class  
- January 18 – Last day to withdraw with refund  
- January 18 – Last day to withdraw with no W posted on transcript  
- January 18 – Last day to apply for Pass/Fail  
- January 21 – Holiday  
- February 4 – Last day to change from credit to audit  
- March 4 – Last day to withdraw  
- March 25-30 – Spring Break  
- April 1-5 – Advising and registration for Summer and Fall 2002  
- April 23 – Last TR class

Final Exam: Tuesday, April 30 – 3:00 PM – 5:30 PM
<table>
<thead>
<tr>
<th>Chapter</th>
<th>Topics</th>
</tr>
</thead>
</table>
| 1       | Structured Design Concepts  
| 2       | Design Tools  
CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools |
| 3       | Basic Features of VHDL  
Major Language Constructs, Lexical Description, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93 |
| 4       | Basic VHDL Modeling Techniques  
Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives |
| 5       | Algorithmic Level Design  
General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems |
| 6       | Register Level Design  
Transition from Algorithmic to Data Flow Descriptions, Timing Analysis, Control Unit Design, Ultimate RISC Machine |
| 7       | Gate Level; and ASIC Library Modeling  
Accurate Gate Level Modeling, Error Checking, Multi-valued Logic for Gate Level Modeling, Configuration Declarations for Gate Level Models, Modeling Races and Hazards, Approaches to Delay Control |
| 8       | HDL-Based Design Techniques  
Design of Combinational Logic Circuits, Design of Sequential Logic Circuits |
| 9       | ASICs and the ASIC Design Process  
What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis |
| 10      | Modeling for Synthesis  
| 11      | Integration of VHDL into a Top-Down Design Methodology  
Top-Down Design Methodology, Sobel Edge Detection Algorithm, System Requirements Level, System Definition Level, Architecture Design, Detailed Design at the RTL Level, Detailed Design at the Gate Level |
| 12      | Synthesis Algorithms for Design Automation  