Due: April 16, 2003

1. Consider the VHDL code below. For the hardware constraint of one adders and two multipliers.
   
a. Draw a data flow graph
b. Derive an ASAP schedule
c. Derive an ALAP schedule
d. Derive a list schedule using the critical path priority metric.
e. Determine a data lifetime chart for the storage elements used.
f. Use the left edge algorithm to obtain an efficient register allocation.
g. Show an allocation diagram for registers and functional units similar to Figure 12.29
h. List all of the hardware elements and quantities needed for this allocation

entity SCHED1 is
  port ( A, B, C, D, E, F : in INTEGER;
             CLK : in BIT;
             X, Y : out INTEGER);
end SCHED1;

architecture HIGH_LEVEL of SCHED1 is begin
  X <= F*(A+B+C*D+D*E);
  Y <= (A*B+E)*D*C;
end HIGH_LEVEL;