Due February 3, 2003

Design a two-out-of five code detector. The device receives as input a 5-bit parallel word. The detector output is a logic 1 for any code word that has exactly two 1’s in it and is a logic 0, otherwise. Model your circuit by performing the following steps.

a. Develop a VHDL entity declaration for the detector.
b. Develop an algorithmic behavioral architectural body for the detector.
c. Develop a data flow behavioral architectural body for the detector.
d. Develop a structural architectural body for the detector.
e. Simulate all three bodies to verify the correctness of each model.

Turn in your VHDL source files and wave and list files.