The University of Alabama in Huntsville
Electrical and Computer Engineering
Project Information
CPE 426/526 01
Spring 2003


Web Page: http://www.ece.uah.edu/courses/cpe526

Instructor: Dr. Rhonda Kay Gaede, Office: EB 211, Phone: 824-6573, email: gaede@ece.uah.edu

Office Hours: MW 4-5, R 9-10, or by appointment

Grading: Homework 15%
Project 25%
Midterm 25%
Final Exam 30%
Class Attendance 5%

Graduate Students will have extra and/or different problems on their tests.

Homework: NO late homework will be accepted without extenuating circumstances. Contact me as soon as a problem occurs.

Important Dates: January 10 – Last day to add a class and file course repeat
January 17 – Last day to withdraw with refund
January 17 – Last day to withdraw with no W posted on transcript
January 20 – Holiday
January 27 – Last day to apply for Pass/Fail
February 3 – Last day to change from credit to audit
March 17 – Last day to withdraw
March 24-29 – Spring Break
April 7 – Advising and registration for Summer and Fall 2003 begins
April 15 – Honors Day – No Classes
April 21 – Last MW class
April 22 – Last day to remedy an I from previous semester

Final Exam: Friday, April 25, 3:00 PM – 5:30 PM

Miscellaneous: Homework will be done individually.
Projects will be done in groups.
Mute your cell phones before you bring them to class.
Both a presentation and a written report are required for the project.

Course Outline:
Chapter 1
Topics
Structured Design Concepts
2 Design Tools
   CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System,
   Simulation Aids, Applications of Simulation, Synthesis Tools

3 Basic Features of VHDL
   Major Language Constructs, Lexical Descriptions, VHDL Source File, Data
   Types, Data Objects, Language Statements, Advanced Features of VHDL, The
   Formal Nature of VHDL, VHDL 93

4 Basic VHDL Modeling Techniques
   Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling
   Combinational and Sequential Logic, Logic Primitives

5 Algorithmic Level Design
   General Algorithmic Model Development in the Behavioral Domain, 
   Representation of System Interconnections, Algorithmic Modeling of Systems

6 Register Level Design
   Transition from Algorithmic to Data Flow Descriptions, Timing Analysis

7 Gate Level and ASIC Library Modeling
   Accurate Gate Level Modeling, Error Checking, Multivalued Logic for Gate
   Level Modeling, Configuration Declarations for Gate Levels Models, Modeling
   Races and Hazards, Approaches to Delay Control

8 HDL-Based Design Techniques
   Design of Combinational Logic Circuits, Design of Sequential Logic Circuits

9 ASICs and the ASIC Design Process
   What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design
   Process, FPGA Synthesis

10 Modeling for Synthesis
    Behavioral Model Development, The Semantics of Simulation and Synthesis,
    Modeling Sequential Behavior, Modeling Combinational Circuits for Synthesis,
    Inferred Latches and Don't Cares, Tristate Circuits, Shared Resources, Flattening
    and Structuring, Effect of Modeling Style on Circuit Complexity

11 Integration of VHDL into a Top-Down Design Methodology
    Top-Down Design Methodology, Sobel Edge Detection Algorithm, System
    Requirements Level, System Definition Level, Architecture Design, Detailed
    Design at the RTL Level, Detailed Design at the Gate Level

12 Synthesis Algorithms for Design Automation
    Benefits of Algorithmic Synthesis, Algorithmic Synthesis Tasks, Scheduling
    Techniques, Allocation Techniques, State of the Art in High-Level Synthesis,
    Automated Synthesis of VHDL Constructs
I promise or affirm that I will not at any time be involved in cheating, plagiarism, fabrication, misrepresentation, or any other form of academic misconduct as outlined in the UAH Student Handbook while I am enrolled as a student at UAH. I understand that violating this promise will result in penalties as severe as indefinite suspension from the University of Alabama in Huntsville.

Signature

Date