Due February 12, 2004

Design a hardware multiplier circuit (M) that computes the product of two, positive 2-bit binary numbers.

A1A0 represents one 2-bit number, B1B0 represents the second 2-bit number and M3M2M1M0 represents the 4-bit product. For example, if A1A0 = 10 and B1B0 = 11, then M3M2M1M0 = 0110. Model your circuit by performing the following steps.

a. Develop a VHDL entity declaration for the multiplier.
b. Develop an algorithmic behavioral architectural body for the multiplier.
c. Develop a data flow behavioral architectural body for the multiplier.
d. Develop a structural architectural body for the multiplier.
e. Simulate all three bodies to verify the correctness of each model.

Turn in your VHDL source files and wave and list files.